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NIST PUBLICATIONS

NISTIR 5851

Project Portfolio FY 1999

Edited by

Stephen Knight
and Alice Settle-Raskin
Office of Microelectronics Programs

U.S. DEPARTMENT OF COMMERCE

Revised May 1999

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Office of Microelectronics Programs

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Foreword

What is the NSMP?

Established in 1994, the National Semiconductor Metrology Program (NSMP) narrows the ever-present gap between the kind of metrology the semiconductor industry needs and what it is able to do. Meeting this challenge is a real feat because the industry tends to outstrip its metrology at every turn. For years, the industry has improved its productivity by a factor of four every eighteen months and it will probably continue to do so. What makes it possible? Continuous improvements in semiconductor processing - such as using ever shorter optical wavelengths to achieve higher circuit densities, increasing the ways that sensors are used to monitor and control chemical and physical processes, and by introducing new process materials into the mix.

Increasing Yield.

The industry counts on the NSMP to support its rate of growth by addressing critical issues and providing timely solutions to show-stoppers, and the NSMP delivers. Projects funded by the NSMP in the last few years have helped industry tighten its controls and increase process yield. In the industry's infancy, the yields at start-up was typically processes that might range from a few percent and would rise to 50 percent at peak production. Today, yields are as high as 80 percent and they can move up to the high 90s when everything's on target.

Paving the Way.

Outcomes from the NSMP which have been of critical importance to the industry include standard reference materials (SRMs®), "NIST-traceable" reference materials (NTRMs®), chemical and plasma reaction kinetics, sensor and instrument calibration techniques, and new metrology techniques. Examples which are used extensively by the semiconductor industry include: NIST SRMs® for bulk resistivity of silicon covering over four orders of magnitude in resistivity; NIST SRMs® calibrated diameter small particles relevant to semiconductor manufacturing; NIST SRMs ® for thin silicon dioxide dielectrics are enabling industry to create larger diameter "NIST-traceable" dielectric film reference materials; chemical and plasma reaction kinetics for chemical species used in semiconductor processing have been and are being published; calibration techniques and calibration services for residual gas analyzers and gas flow meters; data for inert and reactive process gases; a calibration instrument and technique for measuring water vapor in the parts per billion range; techniques for measuring physical and electrical properties of interconnect materials; and techniques and modeling software to extend critical dimension measurements down to the ever-shrinking dimensions of integrated circuit structures. *In short, critical metrology technology developments extend across all the myriad of disciplines required for the semiconductor industry.*

David and Goliath.

The 1997 National Technology Roadmap for Semiconductors, a semiconductor industry-supported technology needs analysis document, highlighted numerous advances in metrology as critical to the continuing success of the industry.

When you consider the scale at which metrology must advance in this industry, the NSMP may seem a bit like David challenging Goliath. To assure that this Program, currently funded at about $12 M with an ultimate funding goal of $25M annually, is responsive to the industry needs, the Office of Microelectronics Programs (OMP) was established. The Program consists of semiconductor metrology projects across most of the NIST laboratories. The OMP matrix-manages the program to achieve maximum results.

Fostering NIST's Relationships with the Industry.

NIST's relationships with the Semiconductor Industry Association (SIA), SEMATECH, and the Semiconductor Research Corporation (SRC) are also managed through the Office of Microelectronics Programs (OMP). Staff from OMP represent NIST on the SIA committees that develop the National Technology Roadmap for Semiconductors as well as on numerous SRC technical management committees. OMP staff also act on behalf of NIST in the semiconductor standards development work of the American Society for Testing and Materials (ASTM), the Deutsches Institut für Normung (DIN), the Electronic Industries Association (EIA), the International Organization for Standardization (ISO), and the Semiconductor Equipment and Materials International (SEMI).

Learn More about the NSMP.

This booklet was prepared to help you to learn more about the 38 projects currently being conducted through the NSMP. In all, they reflect the National Institute of Standards and Technology effort to meet the highest-priority measurement needs of the semiconductor industry. You will see the direct correlation between the gaps in technology expressed by the National Technology Roadmap for Semiconductors and other authoritative industry sources and the focus of this program. It reflects NIST's ability to listen to the needs of industry and to respond with the measurement means to solve the problems. For further information about our program or to let us know your specific questions or concerns, please use any one of the following means to reach us:

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Please note:

Disclaimer: Certain commercial equipment and/or software is identified in this report to adequately describe the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment and/or software identified is necessarily the best available for the purpose.

References: References made to the *National Technology Roadmap for Semiconductors* (NTRS) apply to the most recent edition, dated 1997. This document is available from the Semiconductor Industry Association (SIA), 181 Metro Drive, Suite 450, San Jose, CA 95110, phone: (408) 436-6600, fax: (408) 436-6646.

Appendices: To enable the reader to learn more about the information included in this booklet, we have included appendices toward the back including an acronyms/abbreviations list, a keywords index, and a list of recent National Semiconductor Metrology Program (NSMP) related publications.

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Critical Dimension and Overlay

Nanometer-Scale Dimensional Metrology with SEM and Scanned Probe Techniques

The scanning electron microscope (SEM) is the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. Scanned probe microscopes (SPMs) possess unique capabilities which may significantly enhance the performance of SEMs for in-line critical dimension (CD) measurements. This project utilizes a combined SEM/SPM system to monitor cross-cutting issues such as:

1. **Charging and contamination.** Energetic electrons from the beam penetrate the structures under inspection and interact with the structure and the SEM chamber environment to produce charging and contamination which affect the measurement and cannot be accounted for in modeling. NIST is beginning to address these issues by implementing a combined SEM/SPM system for this purpose in conjunction with a Cooperative Research and Development Agreement (CRADA) partner. There are several directions which this project is currently exploring with this system: An SEM/SPM system was delivered and evaluated at NIST, revealing operational limitations in the current tool. The SEM/SPM was returned for upgrading and some suggestions were implemented by the CRADA partner. During FY99 the upgraded instrument will be evaluated under vacuum and ambient conditions. The remaining limitations which limit the full SEM performance to be achieved are being addressed by the implementation of a novel force sensor based on a quartz microfabricated tuning fork (TF). During FY99 fabrication and operation of the TF sensor on the SEM/SPM instrument will be accomplished as well as on a second SPM available in the laboratory. Manufacturable attachment methods for assembling microfabricated silicon probe tips onto TF sensors has been demonstrated at NIST.

2. **SPM tip stability.** The stability and wear of probe tips depends on the angular orientation of the probe tip to the surface plane of the sample. Misalignment may expose different crystalline regions of the silicon tip, each of which possesses somewhat different mechanical and chemical resistance when in contact with sample material. The combined SEM/SPM provides information about tip wear. These studies will be initiated during FY99 once efficient and reliable operation of the SEM/SPM becomes routine.

3. **Polysilicon gate metrology.** Local electrical characterization of sample surface structures through capacitance and surface potential measurements can provide an entirely new level of understanding of how the level and types of surface defects in silicon and other materials lead to inhomogeneous charging and how the build-up of charge promotes the subsequent growth of hydrocarbon contamination. Electronics needed to perform the electrical measurements will be procured and an operating system demonstrated during FY99.

Metrology is mentioned throughout the Lithography chapter of the 1997 National Technology Roadmap for Semiconductors (NTRS). Requirements are defined on page 94, Table 28. Potential solutions are on page 95, Figure 22. Metrology is cited as one of the grand challenges on pages 11 and 12.

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Nanometer-Scale Dimensional Metrology with Atomic Force Microscopy

Atomic force microscopes (AFMs), which are capable of nanometer resolution, have emerged as important new instruments for semiconductor applications. Among the potential advantages of AFMs are the ability to image features of almost any material and compatibility within the clean room environment. Presently, NIST has a two-element program to extend the technical understanding of AFM and facilitate the application of AFMs in the semiconductor industry. These elements are: (1) the development of a metrology AFM, and (2) collaboration and interaction with industrial users, vendors, and academic researchers on metrology applications of commercial instruments.

First, NIST has constructed a calibrated metrology AFM (C-AFM) with 3-axis interferometric determination of tip position. This is a research instrument specifically designed to aid development of suitable AFM standards, and is capable of nanometer-scale dimensional measurements, with metrology traceable to the wavelength of light in all three axes. Its pitch, height, and width measurement capabilities have been evaluated and validated by internal comparisons. They are presently at or near desired performance levels. Pitches ranging up to 20 μm can be measured, using an edge-to-edge measurement method, with uncertainties (1σ) of ~1.5 nm at sub-micrometer scale and ~0.07% at the largest scales. For measurement of periodic samples, especially holographic gratings, frequency domain analysis of the data allows for further reduction in uncertainty. This is being actively developed to determine the lower limit of C-AFM measurement uncertainty. Step heights ranging from a few nanometers up to several hundred nanometers can be measured with uncertainties (1σ) of ~0.1%. The widths of sub-micron near-vertical features can be measured to an uncertainty (1σ) of ~10 nm to 20 nm, due mostly to the uncertainty in correction for the size of the tip.

Second, the NIST program involves interaction with industrial users and collaboration with academic researchers on AFM metrology. During FY98, our first pitch measurements for an external customer were completed. We quoted, on sub-micrometer intervals, expanded (2σ) uncertainties of about 1% to 2%, with the larger values resulting from sample non-uniformity. Our first step height measurements for an external customer are planned for FY99. Another significant effort involves a collaboration with researchers at the University of Maryland on step height metrology at the sub-nanometer scale. These workers have fabricated silicon samples in UHV with single atomic steps on the surfaces. These types of samples have now been studied by many different investigators and it is widely believed that these samples have considerable potential as fundamental step height. We have performed C-AFM measurements on many such samples, prepared by both resistive heating and electron bombardment, under a variety of measurement conditions. The expected value of the step height, based upon the measured lattice constants of bulk silicon, is about 0.314 nm. The reproducibility of the C-AFM measurement of the step height was observed to be 0.0025 nm. The measured value with the C-AFM, an average resulting from six different sets of twenty subsequent images, is 0.304 nm +/- 0.008 nm. The difference between the measured value and the lattice constant value is almost within the measurement uncertainty. Therefore, we are not presently certain whether or not the native oxide step height differs from the underlying silicon lattice. During FY98 we evaluated and distributed a set of silicon step samples, prepared at the University of Maryland, to our industrial collaborators. The feedback was generally positive, and during late FY98 we began to receive data from some of the participants. During FY99, we will analyze data received from collaborators and make further recommendations to them concerning the best use of the samples and strategies for analysis of the data.

This is a dimensional metrology project, with NTRS references identical to those given for the "Nanometer-scale Dimensional Metrology with SEM and Scanned Probe Techniques" (project # 1).

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Model-Based Metrology

The semiconductor industry requires fully automatic size and shape measurements of very small, 3-dimensional features. These features are currently 180 nm and smaller in size and the measurements must be done in seconds with an accuracy and precision approaching atomic levels. Currently scanning electron microscopes (SEMs) are, and will be for the foreseeable future, used for these measurements. Unfortunately, as SEMATECH and its member companies have determined, the SEM-based dimensional metrology today is not adequate to deliver the high-quality, accurate results needed by today's production requirements. But, it is the only tool available which can handle the needed throughput with an acceptable level of precision. One main problem is that the measurements are done with primitive edge criteria (regression algorithm, threshold crossing) and certain, not necessarily justified presumptions and beliefs. Many times these one-size-fits-all measuring algorithms fail to give acceptable results on the smallest, so-called critical dimensions (CDs) of transistor gate structures.

The images and line scans taken with CD or laboratory SEMs contain much more information that is generally being used: for example these images and the individual line scans differ for "same width" resist lines taken at various focus and dose settings. Beyond the fact that this is a source of measurement error, further information can be extracted, like whether or not the given line was exposed with the intended dose and focus. This information is essential in current and future UV lithography. Modeling the possible cases can help to draw correct conclusions and also makes possible to use more accurate, customized measuring algorithms. Model based metrology is a new concept, which will ultimately combine a number of currently developing areas into a single approach. These five areas are:

- **Adaptive Monte Carlo Modeling.** Adaptive Monte Carlo modeling utilizes a database of measured video waveforms from production samples and compares it to a library of modeled waveforms;

- **Modeling/Image Simulation.** The various new Monte Carlo methods, especially those developed at NIST (MONSEL Series), are providing better and more accurate data than ever. The modeled results are very closely matching the results of real measurements;

- **Specimen Charging.** SEMATECH and the Advanced Metrology Advisory Group (AMAG) has identified charging as the biggest problem in accurate SEM-based metrology and the successful modeling of the geometry of real integrated circuits;

- **Signal Path Modeling.** The modeling of the signal path, including the electronics and signal processing of the SEMs remains a fertile area of research and is critical to the successful development of an accurate model; and

- **Algorithm Development and Analysis.** Algorithms currently used in metrology instruments have no statistical basis for analysis of the data.

Metrology is mentioned throughout the Lithography chapter of the 1997 National Technology Roadmap for Semiconductors (NTRS). Requirements are defined on page 94, Table 28. Potential solutions are on page 95, Figure 22. Metrology is cited as one of the grand challenges on pages 11 and 12.

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Linewidth Correlation

NIST is responsible for providing linewidth SRMs® (standard reference materials) and/or calibration services to meet the needs of U.S. industry. Our current linewidth standards are optically based with a total uncertainty of approximately 37 nm 2σ. As device sizes shrink, the semiconductor industry needs to measure sub-micrometer lines with uncertainties of a few nanometers. The magnetic recording and photographic industries have gap width and grain size measurement requirements at approximately the same scale.

Neither NIST nor any other national laboratory presently offers a linewidth measurement service or SRM with this level of accuracy. The reason is related to a fundamental difference between a width measurement and other kinds of dimensional measurements such as pitch or height. Microscopes produce images which are distorted representations of the specimen. In general, the distortion includes an error in the location of an object's edge. For pitch and height measurements, where the distance is between two edges of the same type (i.e., either both right edges or both left edges for a pitch measurement; both top edges for a height measurement), the bias cancels to first order. As a result, accurate knowledge of the bias is not necessary for this kind of measurement. But linewidth measurement is a left edge to right edge distance determination. Instrumental bias does not cancel, but doubles. Accordingly, physical linewidth determination with any microscopic technique requires modeling of the probe/sample interaction in order to identify edge locations. A barrier to accurate linewidth determination has been acquisition of models in which we can have the required level of confidence.

Linewidth measurement capabilities at NIST span several techniques, including optical, scanning electron, and scanned probe microscopies for physical linewidth as well as electrical techniques to measure the average width of conducting paths. This project seeks cooperative interactions among practitioners of the various techniques. This cooperation includes information exchange among practitioners of the various methods. It includes model development as well as design and execution of experiments for cross-technique comparison of measurements. These intercomparisons serve as a mechanism for cross-checking models and procedures among the different techniques.

As summarized in Table 28 on page 94 of the 1997 NTRS, gate CD control requirements will be below 10 nm within the next few years. This, coupled with the NTRS statement (page 186) that "Uncertainties in the certified value of the reference material must be less than 1/4 of the variability of the manufacturing process to be evaluated or controlled..." places a significant demand on CD (i.e., linewidth) measurement accuracy. Indeed, CD measurement may be one of the areas the NTRS authors had in mind when they wrote (page 186) that "In some areas of metrology no current method of measurement is adequate for the purpose."

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Single-Crystal CD and Overlay Reference Materials

The NTRS projects the decrease of gate linewidths used in state-of-art IC manufacturing from the present 0.25 μm level to 0.09 μm within several years. Scanning electron microscopes and other systems used for linewidth control exhibit measurement uncertainties exceeding NTRS specifications for these applications. These uncertainties could be significantly reduced through the use of reference materials with linewidths certified to nanometer-level levels. Such artifacts are unavailable because the technology has not been developed. The parallel need for certified overlay reference materials is also unserved by any known hardware architecture and test algorithms.

This project consists of five elements: (1) the use of Silicon-on-Insulator (SOI) materials for traceable CD reference-artifact implementation (2) the utilization of electrical-CD metrology for cost management (3) the use of transmission-electron microscopy for traceability (4) application of similar techniques for the fabrication and certification of overlay reference materials.

Prototype SIMOX/SOI test chips have already been distributed to a consortium of eighteen semiconductor manufacturing companies In several cases, the differences between electrical CD, SEM, and AFM measurements were systematically below approximately 20 nanometers. Based on Consortium-members' recommendations, the project introduced a new test-chip design replicated on BESOI material. These chips will be ready for distribution during the current year after necessary analyses of electrical test data are completed.

The significant reduction of CD-measurement divergence that has been observed with the SOI implementations is attributed to its unique physical properties. However, the critical issue of accuracy requires traceability to fundamental physical constants. The project is developing an "atomic ruler" based on the known spacings of silicon lattice-planes. A method of extracting reference-feature linewidths by high-resolution transmission-electron microscopy (HRTEM) is being developed to provide the necessary traceability path. Reduction-to-practice will be demonstrated by the end of the year. Establishing a commercial supply of certified reference materials to industry is being studied in collaboration with a leading standards supplier.

The routine use of HRTEM for traceability purposes has been found to have too high a unit cost. A secondary reference means that may be calibrated by HRTEM is desired. It must exhibit nanometer-level reliability, low cost, and a level of robustness that is not provided by any technique other than electrical CD metrology. During 1999, a method of co-extracting electrical and HRTEM CDs from the same reference features is being implemented.

A novel wafer-fabrication process for enabling direct estimates of tool-induced overlay shifts has been developed. We are currently refining the process to allow certification by electrical means. Interconnect edge-detector wafer lots for process-specific shift extraction are in progress. At year's end we will have sample artifacts of both types ready for distribution to industry for field testing.

This is a dimensional metrology project, with NTRS references identical to those given for the "Nanometer-Scale Dimensional Metrology with SEM and Scanned Probe Techniques" (project # 1) . The 1997 NTRS discusses overlay and CD metrology and the associated roadblocks in the Section on MICROSCOPY on page 182. The challenges confronting NIST, which are addressed by this project, are on reviewed un the section on REFERENCE MATERIALS" on page 186.

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Atom-Based Dimensional Metrology

The goal of this project is to develop three dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable to allow transfer to other measurement tools which can measure the artifacts with dimensions known on the nanometer scale.

There is a demonstrated need by the semiconductor industry for measurement methods and artifacts whose dimensions are known with nanometer scale accuracy. Measuring linewidth structures accurately at these small feature dimensions is difficult as evidenced by the lack of industry standard artifacts. This project is developing methods and artifacts whose feature dimensions are known on the atomic scale. These artifacts, known as atom-based standards, are artifacts whose edge locations can be determined [e.g. using a Scanning Tunnel-in Microscope (STM)] to atomic dimensions and whose lateral dimension is based on the metric of the crystal lattice. These samples, once atomically characterized, can then be used in several applications to calibrate secondary standards, actual metrology tools in the fab, or other standards metrology tools at NIST.

NIST has developed the means for the production of known reproducible STM tip shapes, the accurate measurement of tip geometry, and models which interpret imaging data to extract real feature dimensions. We are currently having fabricated a new set photolithographically patterned three-dimensional structures in semiconductor materials. We are also developing the methodology to enable the transfer of atom-counted samples to other measurement tools such scanning electron microscopes or atomic force microscopes.

The development of artifacts with photolithographically defined features is proceeding in both silicon and GaAs semiconductor materials. Each of these materials is being pursued in parallel as potential atom based standards materials. Both can be photolithographically patterned and have surfaces which can be atomically reconstructed. For artifact fabrication, we are working with several manufacturers in the semiconductor industry for our silicon processing while for the GaAs patterning we are collaborating with EEEL.

We have used the UHV Prep Chamber for preparation of long range atomically ordered silicon surfaces. Additionally, we have prepared long range atomically ordered GaAs surfaces. Successful methods have been develop for STM tip fabrication and analysis by UHV field evaporation including high resolution CCD image analysis now being used to capture and analyze FIM images. Current work is focused on developing preparation methods for atomically ordered surfaces on etched features. The integrity of the etched linewidth features is a paramount concern when preparing features with long range atomic order.

This is a dimensional metrology project, with NTRS references identical to those given for the "Nanometer-Scale Dimensional Metrology with SEM and Scanned Probe Techniques" (project # 1) . The 1997 NTRS discusses overlay and CD metrology and the associated roadblocks in the Section on MICROSCOPY on page 182. The challenges confronting NIST, which are addressed by this project, are on reviewed un the section on REFERENCE MATERIALS" on page 186.

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Optical CD and Overlay Metrology

Tighter tolerances on CD measurements in wafer production place increasing demands on photomask linewidth accuracy and on overlay tolerances. NIST has a comprehensive program to both support and advance the optical techniques needed to make these measurements.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch artifacts in the range of 0.5 μm to 30 μm are currently certified on a green light optical calibration system. Linewidth uncertainties have been reduced to 40 nm. These standards are being compared with linewidth measurements in other national standards laboratories.[1] An ultraviolet transmission microscope has been constructed that will replace the green light system. This new instrument uses a unique geometry (a Stewart platform) as the main rigid structure and shows considerable improvement in vibration characteristics over a conventional microscope. Reduced transmission of UV through the chrome and reduced instrument vibration will offer improved linewidth uncertainties.

To meet the future challenges in overlay metrology, a state-of-the-art reflection mode confocal microscope has been constructed at NIST. This instrument also utilizes a Stewart platform, three-axis interferometry monitors sample position, and a collimated laser beam monitors stage tilt. The optical resolution is nominally 0.25 μm. A CCD camera and image acquisition electronics enable general use of the instrument in reflection mode on semiconductor samples. The overlay metrology program is investigating and developing a new set of overlay standards. These standards consist of artifacts which will allow users to align their overlay instrument properly and minimize tool-induced shift. Currently under development is the stepped microcone alignment artifact.[2] In parallel with the stepped microcone is a two-dimensional scale calibration standard also intended for use in instrument alignment. Prototypes of both artifacts have been fabricated. A series of measurements are currently underway with industry collaborators to improve artifact design and validate analysis capabilities. We are also in the fabrication phase with SEMATECH for a complete set of conventional overlay target structures covering most of the commonly used target geometries and dimensions. These targets, to be developed into standard reference artifacts, will be available at least at two different process levels. Modeling and simulation efforts continue with investigations into material and geometry related issues with an emphasis on improving measurement repeatability, accuracy, and ensuring a broad enough parameter space for useful calibrated conventional overlay patterns.

Two dimensions of interferometry on the overlay metrology tool are operational with a VXI/VME control system. The system can acquire data in an interferometric mode or in a full CCD array mode. These data are then be analyzed using Matlab based image analysis and signal processing code developed in-house. Prototype stepped microcone artifacts have been successfully fabricated and measured. Significant progress has been made in detailed experimental/model and model/model comparisons under a joint SEMATECH/NIST venture to improve simulation and modeling tools through a series of computer code improvements and extensive measurements using the overlay tool. A quantitative analysis of the overlay system is in progress in conjunction with new developments in auto-focus algorithms and improved edge detection. NIST optical overlay personnel are additionally involved in several industry collaborations with SEMI, SEMATECH, IBM, Hewlett Packard, Photronics, KLA/Tencor, Schlumberger, and several others in the design and development of overlay metrology tool alignment structures and conventional overlay target structures to be calibrated at NIST.

NIST is also developing a magnification standard for optical microscopes (SRM 2800) with certified pitch patterns from 1 cm to 1 μm produced on standard size slides. In addition, NIST has outlined a new technique for measurement of photomask linewidths called Emulated Stepper Aerial Image Measurement.

This is a dimensional metrology project, with NTRS references identical to those given for the "Nano-scale Dimensional Metrology with SEM and Scanned Probe Technique" (project # 1).

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[1]Potzick, J. and Nunn, J., International comparison of photomask linewidth standards: NPL-NIST, Proceedings SPIE 2725-08: 124-129.

[2]Silver, R. M., Potzick, J., Scire, F., Evans, C., McGlaughlin, M., Kornegay, E. and Larrabee, R., A method to characterize overlay tool misalignments and distortions," Proceedings SPIE 3050: 143-155.

High-Accuracy Two-Dimensional Measurements

The ability to place features accurately in 2D has multiple impacts in the electronics industry. The situation regarding this critical capability is unusual in that state-of-the-art commercial measuring machines are so accurate that there is no available source of better 2D measurements from which standards can be established. As such, each user's measurements today are traceable only to one particular measuring machine. NIST clearly recognizes the industry-wide exposure inherent in this situation and is developing innovative approaches to solve the problem.

We have begun, in conjunction with Dr. Richard Silver of the Precision Engineering Division, a plan to work with industry to develop a standard grid which will be sold as a NIST Standard Reference Material to standardize 2D measurements in the semiconductor industry. The program has three main parts: development of a industry consensus standard grid, measurements by state-of-the-art measuring machines in private industry, and verification of the measurements using NIST capabilities. A prototype grid has been made and measurements begun. Each measurement of the grid will have data in each of at least two orientations. Rotating the grid 90 degrees between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the straightness of each machine axis travel.

Verification of the grid measurements will be made at NIST. The overall scale of the grid will be checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1D measurements available in the world. We will begin an effort for straightness measurements using the M48 coordinate measuring machine and a high accuracy straight edge. Combining our tools for centering on the grid marks, and earlier work on straight edge reversal techniques, we will be able to measure the straightness of each line of grid marks to a few nanometers. Since the linescale and M48 have 1 meter or more of travel, the measuring systems will be available to measure 300 mm reference plates when they are needed in industry.

Finally, the long term solution for industry is to develop suitable self-calibrating measurement algorithms. We have had one SBIR grant to implement the most advanced algorithm for the self-calibration of measuring machines with grid plates, and are working with another company through the SBIR program to design, implement, and test new algorithms.

Two-dimensional measurements are implicitly needed for controlling overlay capabilities of steppers and mask-making tools. Overlay is listed in Table 23, page 83 of the 1997 edition of NTRS as a difficult challenge for both >100 nm and <100 nm processes and states that overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 100 nm. Also overlay over large field sizes will continue to be a major concern for sub-130 nm lithography. It also shows, in Table 26, page 87, that two-point placement accuracy is and will be a critical issue for rules at 180 nm and less.

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Two- and Three-Dimensional Dopant Profiling

Scanning Probe Microscopy for Dopant Profiling

NIST is developing the Scanning Capacitance Microscope (SCM) and related software analysis tools for measurement of two-dimensional (2D) dopant/carrier profiles in silicon. The National Technology Roadmap for Semiconductors (NTRS) projects the need for a dopant-profiling tool capable of 4% precision in dopant concentration and 3-nm spatial resolution in the year 2001. The project has two elements: 1) Development of accurate SCM models and theoretical understanding; and 2) Improvement of the practical metrology aspects and usability of the SCM. The dopant profiles in silicon transistors largely determine the performance and hot-carrier reliability of modern devices. Precise and accurate measurements of 2D dopant profiles in silicon could be used to calibrate technology computer-aided design (TCAD) simulations of the dopant profile produced by specified fabrication processes. Current efforts in the project seek to correlate 2D carrier profiles measured with the SCM with TCAD simulations of dopant/carrier profiles fabricated using the same process parameters.

We have developed software that readily extracts 2D carrier profiles from SCM images of dopant gradients in like-type silicon substrates. While the SCM can image cross-sectioned transistors containing p-n junctions, extraction of high confidence 2-D carrier profiles from these images remains elusive. Real devices containing p-n junctions cannot be precisely interpreted with the models developed for dopant gradients in like-type silicon. Extensive Finite Element Method simulations of SCM images including a realistic tip shape across p-n junctions are underway. Last year, this work resulted in a practical technique to determine the electrical junction location in SCM images. We are developing practical measurement procedures and models to extract carrier profiles from SCM images that contain p-n junctions and steep dopant gradients.

For the SCM technique to meet the NTRS dopant profiling goals, it must be possible for industrial users to convert reliably measured SCM images to 2D carrier profiles. The NIST SCM models have been integrated into our *FASTC2D* SCM image-to-carrier profile interpretation software. *FASTC2D* utilizes a database of calculated SCM capacitance-voltage (C-V) curves to rapidly convert SCM signal to an equivalent carrier concentration. *FASTC2D* extracts the carrier profile from an SCM image in less than 1 minute. A preliminary version of *FASTC2D* for personal computers is now available to industrial partners for evaluation. Feedback on the usability of *FASTC2D* from industrial partners will be incorporated into the first published version to be available later this year.

To become an accepted tool, SCM must demonstrate its spatial resolution, dopant concentration precision, and reproducibility. We have entered a phase of working with industrial partners to develop standard test methods and to demonstrate site-to-site comparability of SCM measurements.

We are also developing other scanning probe microscope techniques to determine the spatial variation in the electrical properties of semiconductors. We have developed the intermittent-contact mode of the SCM (IC-SCM) as a technique which is sensitive to variations in the dielectric constant of thin films. Since the IC-SCM can detect metal lines buried beneath planarized insulating layer, it also has potential applications for determining lithographic overlay. Optically-pumped SCM is being developed as a tool to investigate spatial variations in carrier lifetime in a silicon wafer.

The 1997 NTRS lists 3D dopant profiling as one of the five most difficult future metrology challenges in Table 28 with performance goals listed in Table 29. SCM and SPM based techniques for dopant profiling are discussed in the Metrology section; and for overlay measurements in the Lithography section.

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Thin-Film Profile Measurement Methods and Reference Materials

NIST is pursuing a multifaceted analytical approach to 2D and 3D compositional profiling. Main objectives of this work are to: (1) define optimum procedures for ultra-high depth resolution and ultra-shallow profiling by Secondary Ion Mass Spectrometry (SIMS); (2) develop depth-profiling reference materials to assist the semiconductor industry; and (3) develop methods to improve the uncertainty of implant dose measurements by SIMS.

For ultra-high depth resolution profiling, we have explored the use of a rotating SIMS sample stage to minimize sputtering-induced roughness as a factor in depth resolution. A large improvement in the profiling of metal multilayers has been demonstrated. We are also studying the use of novel primary ion beam species in commercial SIMS instruments to improve depth resolution. Working with a U.S. instrument manufacturer, a filament-based duoplasmatron ion source has been developed to produce molecular ion beams such as SF_5^+ with sufficient beam current to be practical for depth-profiling applications. This species produces much less sub-surface rearrangement of the sputtered sample than do more conventional ion beam species such as O_2^+ or Ar^+. We have used this source during FY98 to profile ultra-low energy boron implants and delta-doped boron layers in silicon. At similar bombardment energies, the SF_5^+ profiles show markedly improved depth resolution compared with conventional O_2^+ profiles. During FY99 we intend to collaborate with SEMATECH on a more detailed evaluation of this source. We will also investigate a negative cluster ion source based on cesium bombardment for high resolution profiling, and a recently installed TOF-SIMS that has the capability to monitor elemental contamination at interfaces during a depth profile.

NIST has developed two ion-implanted Standard Reference Materials for SIMS calibration, SRM 2137 (boron implant in silicon), and the recently completed SRM 2134 (arsenic implanted in silicon). We will investigate certification methods for a new phosphorus implant SRM during FY99, based on radiochemical neutron activiation analysis. This project will be more challenging than the other two because a chemical separation is an additional required step before counting the beta particles emitted from the activated ^{32}P. A prototype depth resolution reference material for SIMS will also be tested during FY99.

NIST recently collaborated with Lucent Technologies to study the limits of implant dose measurements that are possible by SIMS. The boron doses of three implants of BF_2 in silicon, in nominal 5 % steps, were measured independently by SIMS at the two laboratories, each using carefully designed measurement protocols that incorporated the previously developed NIST boron-implant-in-silicon SRM for dose calibration. Both labs could correctly distinguish the dose order of the three samples; the average dose disagreement between the labs was 1.3 %. Further comparisons are planned during FY99 to assess the level of agreement that can be achieved for arsenic implants using SRM 2134 for dose calibration.

The need for improved SIMS capabilities for ultrashallow doping profile measurements and offline doping process control is discussed in the 1997 NTRS under Process Integration, Devices, and Structures, page 58, under Front End Processes, page 80, and under Metrology, page 181 (Table 61) and page 185 (Figure 48). Requirements of reference materials are discussed in general on page 186.

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Thin Film and Defect Characterization

Metrology of Alternative Gate Dielectrics for CMOS Technology

The 1997 *Semiconductor Industry Association National Technology Roadmap for Semiconductors* (SIA NTRS) indicates that at the end of the roadmap, by the years 2006-2009, the equivalent thickness of the gate dielectric will need to be approximately 1.0 nm or below. Due to increased power consumption and device and circuit instabilities associated with SiO_2 of this thickness, a high permitivity gate dielectric (e.g. Si_3N_4, Ta_2O_5, TiO_2, BST) with low leakage current and at least equivalent capacitance, performance and reliability will be required. The elements of this program are to: (1) provide an understanding of the electrical characterization methodologies required for alternative gate dielectrics for CMOS technology and (2) provide techniques and data for the comparison and development of alternative gate dielectrics fabricated throughout the research community.

Electrical characterization methodologies will be analyzed and developed to address issues associated with these films including leakage currents, quantum effects, thickness dependent properties, large trap densities, and transient behavior. Conductance and capacitance measurements of MOS capacitors with tunneling dielectrics have been examined to properly extract device properties including interface defect densities. In FY 1999, the application and limitations of these measurements on alternative dielectrics such as TiO_2, Ta_2O_5 and Si_3N_4 will be examined using simulations and experiment. Other electrical characterization techniques such as charge-pumping will be investigated. Studies on tunneling, leakage and reliability mechanisms will also be initiated.

Internal and external collaborations are being developed to increase the understanding of the relationship between the gate dielectric material/interface and device electrical measurements. This understanding will be used to provide an improved basis for comparison and development of various measurements and dielectrics. Device samples have been obtained from several university and industry research groups. The plans for FY 1999 are to compare defect densities of alternative dielectrics (e.g. Si_3N_4, TiO_2, Ta_2O_5) measured using several techniques and to further the understanding of the relationship between these results and physical metrology.

"Although there are many challenges facing front end processing there do not appear to be fundamental limits on device scaling to the 100 nm technology generation. However, due to fundamental limits such as tunneling currents, scaling bulk CMOS devices beyond 100 nm will require new materials for the gate dielectric (high k) and gate electrode (metals) as well as new device structures, such as fully depleted silicon on insulator (SOI) and elevated source/drain structures. These are critical showstoppers if not solved." (1997 NTRS, p. 59).

"No suitable alternative high dielectric constant material has been identified with the stability and interface characteristics to serve as a gate dielectric. Years of research and development are required to identify and qualify a suitable alternative material," (1997 NTRS, p. 71).

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Measurements and Standards for Thin Dielectric Films

The decrease of the gate dielectric film thickness to an oxide-equivalent value of 1nm has been identified as a critical front-end technology issue in the NTRS. Oxides will be replaced by dielectric stacks utilizing silicon oxides and nitrides and binary or ternary metal oxides requiring one or two monolayers of interface dielectric using fabrication processes as yet unspecified. The knowledge base needed for high speed, non-contact metrology, such as ellipsometry, to analyze and control the thickness of such complex films at the 0.1 Å level is not yet in hand. This project is focused on the issues of identifying structural models and developing optical constants for improved ellipsometric analysis of such film systems, relating optical, electrical and physical measurements of thickness and developing and providing the basis for traceability of film thickness measurements to NIST. Project tasks include:

1. **Developing optical models and constants for in-line ellipsometry.** We use a custom high accuracy spectroscopic ellipsometer and are collaborating with SEMATECH, member companies and universities in the analysis of advanced oxynitrides, oxide/nitride stacks and metal oxides such as tantalum pentoxide and titanium dioxide. This work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion models for analysis and control of current and potential gate films by ellipsometry in the 1.5-6 eV range.

2. **Optical index of ideal silicon based materials at elevated temperatures.** A custom-built UHV chamber with spectroscopic ellipsometer has been established. Initial verified capability extends to 450C and a 2 to 4eV measurement range.The instrument is being applied to generating the world's best optical index values for true bulk silicon at room temperature; it will be extended to a temperature of 450C for silicon and for dielectric films important for silicon gate technology to enable in-situ control for low temperature processes. Extension of this work to nearly 1000C and an energy range of 1.5-5 eV will depend on success of the initial phase.

3. **Relation of optical, electrical and physical measurements of thickness.** Collaborations have been developed for comparison studies of diverse measurements of thin dielectric films to assess the accuracy of ellipsometric measurements. Initial work showed X-ray, neutron and ellipsometry agreement within 0.1nm for a 10nm SiO2 film. Comparison studies of more complex films with thicknesses to 0.2nm are in progress. State-of-the-art C-V and I-V measurement capability for gate films has been established. Advanced analysis software from commercial, and university sources is being established to determine the effect of model sophistication on thickness values calculated from electrical data. A two-terminal electrical evaluation of buried interface roughness is being extended to 0.25μm n-channel devices. Results indicate that this technique has a lower limit of roughness determination of about 0.1nm with present magnetic field capability.

4. **Establish and transfer basis of accuracy for thin dielectric films.** Industry requirements for future thin film standards were established at a NIST sponsored workshop. Core ellipsometry measurement capability is being expanded and strengthened to meet these requirements. Procedures are being developed to enable traceability to NIST for suppliers of secondary thin-film reference materials without volume production of NIST SRMs. Completion of a NIST-VLSI Standards Inc. CRADA has enabled VLSI to offer NIST traceable standards down to 4.5nm

Thin Film processes and requirements are discussed in the Front End Processes of the NTRS, pp. 71, 72, 79,80,81, Table 22, Fig.16. Associated metrology requirements and reference materials are discussed in various sections, pp. 50, 79,80, 178, 181, 186.

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Thin Film Reference Materials and X-Ray Metrology for Microelectronics

Our program develops and applies X-ray methods to reveal the microstructure of thin film and multi-layer structures produced by advanced semiconductor manufacturing. We also generate and test reference film structures for the calibration of in-line production tools. The main components of this work are the following: (1) Development and application of high-resolution X-ray diffraction techniques; (2) Advanced application of modeling methods to describe specular and diffuse scattering; (3) Production of reference samples of thin film and multi-layer structures; (4) Rapid response to urgent problems identified by SEMATECH.

X-ray probes are characterized by their short wavelengths, the ease with which they penetrate thin film structures, and the slow variation of their interaction coefficients with elements. Their phase velocity in solids differs only slightly from that in vacuum, allowing robust geometric metrology of thin layer stacks. The enumerated program elements have the following contents:

1. **High-resolution X-ray methods.** A new high throughput large capacity diffractometer was built and commissioned in the previous fiscal year. This automated apparatus can accommodate 200 mm and 300 mm wafers, and has advanced beam preparation optics that offer combinations of resolution and flux optimized to specific applications.

2. **Advanced modeling methods.** Our original modeling software (developed in-house) has now been augmented by several public domain and commercial analysis packages. The problem of assigning meaningful uncertainties to the model parameters emerging from the fitting procedures needs attention. A highly qualified scientist will join this effort if support can be obtained for his participation.

3. **Production of reference samples.** We have established a reference materials production capability based on a highly developed ion beam sputtering apparatus. This facility produces single layer samples and multi-component multi-layer stacks with atomic scale resolution and reproducibility. In the last fiscal year, a second sputtering chamber was added which has the capacity to produce uniform coatings on 200 mm wafers. The structures produced in this facility have sufficiently high quality that, after X-ray charcterization, they can be used as reference samples for other thin film measurement systems including those based on ellipsometry, and ultrasonic propagation. Over 30 materials are available for production of complex reference structures.

4. **Rapid response to urgent problems.** Our development of improved measurement and production capability has been staged so as to maintain rapid and effective response to urgent industrial needs. Among the systems we have addressed in this context are: advanced oxynitride dielectrics, TaN copper diffusion barriers, high-k materials such as tantalum pentoxide and barium strontium titanate, and TiN.

The need for improved measurements and reference materials for very thin films is evident in several sections of the 1997 NTRS. By way of example, page 11 indicates the need for gate dielectrics with equivalent oxide thicknesses below 2 nm. Addressing the variety of high K dielectrics, metal interconnects, and barrier layers is facilitated by the ease with which X-ray methods adapt to new systems. Details can be seen in the section on Front End Processes (p 59 & 68). The need for reference materials is emphasized in the Metrology section (p 173 & 174).

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Compositional Metrology for Next Generation Gate Stack Materials

The NTRS projects that gate dielectrics with oxide equivalent thickness to 1 nm or below will be required in the N+2 or 3 technology nodes. To achieve the necessary electrical performance of CMOS transistors several materials and structures are under investigation. Several high dielectric constant materials, e.g., silicon oxy-nitrides, nitride-oxide stacks, barium strontium titanate (BST), tantalum oxide, aluminum oxide, are candidates. Currently analytical methods at the thickness levels necessary for desired transistor performance are not available to support both process development and production metrology needs.

During this coming year, we will conduct a feasibility study of the analytical methods necessary to produce and characterize thin film reference materials typical of next generation gate materials. BST is one of the leading candidate high-κ gate dielectric materials and has been selected as the material for use in this study.

Our program efforts include:

1. **Production of BST Thin Films.** The Ceramics Division, which is in the Materials Science and Engineering Laboratory (MSEL), will develop a metalorganic decomposition (MOD) technique for fabricating BST thin films of varying thickness. Initially, ~ 1000 Å thick, stoichiometric BST films will be deposited on silicon wafers. Once the deposition process has been optimized, thinner films of varying composition will be produced. In addition, BST films may be fabricated in existing metalorganic chemical vapor deposition and pulsed laser deposition facilities, which have been used for the past several years to deposit barium titanate films. The Ceramics Division currently has BST films of varying thickness (300 Å to 1000 Å) obtained from outside sources for various measurement studies; these films will be used in the initial compositional analysis studies described below until in-house fabrication capabilities are developed.

2. **Compositional Analysis of BST Thin Films.** The Surface and Microanalysis Science Division, which is in the Chemical Science and Technology laboratory (CSTL) will use its state-of-the-art, thin-film compositional analysis capabilities to investigate the feasibility of making definitive composition measurements of 10 - 50Å BST films. The analytical work will begin with the existing BST films from MSEL and will progress to thinner BST films as the critical measurement parameters are defined and analytical procedures developed. Various electron probe-based microanalytical methods will be used to obtain quantitative results while investigating issues necessary to obtain high accuracy composition measurements of increasingly thinner layers. Many of the existing analytical correction procedures currently used for analysis of thin films such as multiple-voltage EPMA, AEM/EDS and EELS, low voltage probe analysis, and Auger spectroscopy must be significantly modified to obtain accurate quantitative results on the candidate systems. The film samples fabricated by MSEL will provide the means to investigate the analytical correction procedure modifications necessary and to investigate realistically achievable accuracy levels.

Electron beam microscopy and characterization needs are discussed in the 1997 NTRS on pages 182, 185, and in Figure 48 on page 185. Thin film metrology needs are covered on page 79 of the 1997 NTRS. High κ gate materials are discussed on pages 45,59, 80-81 and in figure 24 on page 104.

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Ultra-Thin Dielectric Reliability Metrology

As the semiconductor industry continues to scale device dimensions to achieve channel lengths below 100 nm, gate dielectrics must be scaled to have an equivalent thickness at or below 1 nm. The reliability of gate oxides is becoming a critical concern as oxide thickness is scaled below 4 nm in advanced CMOS technologies where devices will operate with higher gate electric fields and direct tunneling currents passing through the gate dielectric. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. The project consists of two elements: (1) Improved physics and characterization of time-dependent dielectric breakdown of ultra-thin gate oxides and (2) Development of highly accelerated gate oxide integrity (GOI) test standards through EIA/JEDEC and ASTM international standards organizations.

1. This element focuses on the physics of failure and the reexamination of traditional reliability testing techniques of ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. In FY98 a technique was developed that allows critically important field acceleration parameters and thermal activation energies required for reliability extrapolation to be extracted from very fast highly accelerated oxide breakdown tests. The technique can be applied to tests routinely used in production monitoring and saves over an order of magnitude in testing time. The technique was applied to test data obtained from 3 nm thick SiO_2 films. In FY99 the physical mechanism responsible for "soft" or "quasi" breakdown modes and its implications for device reliability will be investigated as a function of test conditions and temperature. Long-term time-dependent-dielectric breakdown tests will be conducted on SiO_2 films as thin as 1.5nm at lower electric fields closer to operating conditions. Experiments will be conducted to investigated the differences of gate oxide breakdown and wear-out due to high oxide field and hot-carrier injection. This study will provide insight into the physical mechanism of ultra-thin gate oxide wear-out and breakdown.

2. Highly accelerated breakdown tests used as production monitors must also be reevaluated for ultra-thin gate oxides. Traditional ramped voltage and current breakdown tests are not able to detect breakdown in films less than 4 nm thick. In FY98 a new voltage ramp technique has been developed through a SED coordinated collaboration between JEDEC and ASTM. A round-robin was planned and initiated to evaluated the new test. Twelve laboratories are participating. In FY99 SED will continue its leadership role in the JEDEC and ASTM standards committees to develop a new constant voltage breakdown test that is used during process qualification. The new test will utilize noise detection as a means to detect breakdown in films as thin as 2 nm. The voltage-ramp round-robin will continue through FY99.

Thin gate dielectrics for future device scaling is regarded as one of the most difficult challenges by the 1997 NTRS (p. 71). The effect of high tunneling currents on device reliability must be understood as indicated on p. 192 (1997 NTRS), "For 100 nm devices and below, the gate dielectrics will be so thin that gate current will become a very important design factor. Improvements in basic understanding are needed, including reliability aspects". It is also recognized by NTRS that the integrity of the ultra-thin gate oxide is a key reliability issue. "Below 180 nm, the key reliability issues will be the quality of very thin gate oxides" (p. 55). "At 100nm Tox is expected to scale to 2.0 nm. For thin nitrided oxide a key challenge will be understanding the mechanisms of basic oxide conduction and reliability wear-out failure potential", (p.56).

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Chemical Characterization of Thin Films and Particle Contaminants

The 1997 NTRS outlines chemical metrology requirements, including elemental composition, crystallographic phase, chemical structure of microelectronic components and particle contaminants at or approaching nanometer spatial resolution. To meet the needs implied for the development of next-generation devices, we must significantly improve the spatial resolution, analytical sensitivity, and accuracy of our chemical measurement capabilities as well as the production of related standards. We are addressing the NTRS chemical measurement challenges through several efforts. First, we are investigating the application of a wide range of existing instrumentation, such as transmission and scanning electron microscopy and electron probe microanalysis, expanding their capabilities to meet the analytical requirements for advanced devices. Second, we are developing and testing analysis methods that are based on new chemical measurement technologies such as the X-ray microcalorimeter detector, high speed silicon drift detectors, backscattered electron diffraction (BSED), and grazing incidence X-ray photoelectron spectroscopy (GIXPS) to determine their accuracy, sensitivity, and spatial resolution. Finally we are developing analytical standards in support of these measurements efforts.

Our program efforts include:

1. **Transmission Electron Microscopy.** The TEM allows direct imaging and analysis of the complex interlayered structures composing microelectronic devices. We are applying elemental analysis using Electron Energy Loss Spectrometry (EELS) and X-ray spectrometry combined with near atomic resolution imaging of cross sections to characterize devices. This years investigations focused on silicide formation in $Co/Si_{1-x}Ge_x/Si$ mulitlayers grown by molecular beam epitaxy. High-resolution X-ray and EELS maps were used to characterize silicide reaction products, important in the development of $CoSi_2$ contacts in $Si_{1-x}Ge_x$ devices.

2. **Electron beam Particle Analysis.** Particle contaminants during device manufacture are a significant source of device failure. Characterization of particle composition allows the fabrication facility to identify and control the particle source. This year, we have used BSED to identify the crystallographic phase of submicrometer particles and have investigated the effect of using low voltage X-rays to improve quantitative elemental analysis of particles. In addition, we are investigating high-resolution low-energy X-ray analysis with the NIST microcalorimeter X-ray detector, and high speed automated analysis with silicon drift detectors.

3. **GIXPS.** GIXPS is used to explore chemical bonding with nanometer spatial resolution. Taking measurements at various grazing angles of the incident X-ray beam allows GIXPS to map the chemical bonding of a device as a function of depth. This year we have used GIXPS to analyze successfully SiO_2 films as thin as 1.4 nm on Si as well as a 0.2 nm carbon surface layer on the SiO_2 film.

4. **Standards.** Thin film and particle standards play a critical role in the development of the various chemical measurement technologies. This year we have completed a series of measurements on a candidate SRM, Thin Film Steel, and a TiN thin film on Si RM. These materials a scheduled for release this coming year.

Electron beam microscopy and characterization needs are discussed in the 1997 NTRS on pages 182, 185, and in Figure 48 on page 185. SOI technology needs are covered in the 1997 NTRS on pages 60 and 62, and in Table 19 on page 60. Thin film metrology needs are covered on page 79 of the 1997 NTRS.

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High-Resolution Microcalorimeter X-Ray Spectrometer for Chemical Analysis

Improved X-ray detector technology has been cited by SEMATECH's Analytical Laboratory Managers Working Group (ALMWG) as one of the most important metrology needs for the semiconductor industry. In the Metrology Roadmap section of the 1997 National Technology Roadmap for Semiconductors (NTRS), improved X-ray detector technology is listed as a key capability that addresses analysis requirements for small particles and defects. The transition-edge sensor (TES) microcalorimeter X-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers (EDS). At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 mm to 0.3 mm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. With commercialization and continued development, microcalorimeter EDS should be able to meet both the near-term NTRS goal of analyzing particles as small as 0.08 mm in diameter and the longer-term requirements of the semiconductor industry for improved particle analysis.

The microcalorimeter EDS has an energy resolution at least 10 times better than semiconductor EDS and comparable to that of cumbersome wavelength-dispersive spectrometers (WDS). Over the past year, other performance features of microcalorimeter EDS have been improved to approach that of high-resolution semiconductor EDS in terms of solid angle (7 msr using a polycapillary optic X-ray lens) and maximum count rate (500 s^{-1}; over 1000 s^{-1} using a beam-blanker). The excellent energy resolution of our "general purpose" microcalorimeter EDS (~10 eV FWHM over the energy range 0 keV to ~10 keV) allows straightforward identification of closely spaced X-ray peaks in complicated spectra, including overlapping peaks in important materials (such as TiN and WSi2) which cannot be resolved by semiconductor EDS. We have also developed a TES microcalorimeter with an instrument-response energy resolution of 3.1 eV ± 0.1 eV FWHM (digital processing) and ~4 eV FWHM (analog processing) over the energy range 0 keV to ~2 keV which is particularly appropriate for particle analysis. It is clear, however, that the fundamental limits of this type of detector have not yet been reached. In the next year, it is anticipated that both energy resolution and speed can be improved through development of new photolithographic fabrication methods for the detectors.
Using our dedicated microcalorimeter EDS/SEM system, we have demonstrated particle analysis of 0.3 μm W particles and 0.1 μm Al_2O_3 particles on Si substrates, both difficult identification problems. In particular, the analysis of the W particles is not possible using conventional semiconductor EDS detectors due to the severe peak overlap between the Si-K and W-M lines, which is easily resolved using the microcalorimeter EDS. With improvements in the entire detector system (both SEM and spectrometer), it is anticipated that the NTRS goal of identifying 0.08 μm particles should be achievable in the near future.

The improved energy resolution of the detector has also enabled the use of the microcalorimeter spectrometer to observe shifts in the spectra of elements depending on their chemical bonding state. By carefully calibrating the response of the detector, chemical shifts between Al and Al_2O_3 and between Fe and Fe_2O_3 were measured. Because the shift in energy due to chemical bonding is small (on the order of an electron volt), such observations are impossible with conventional semiconductor EDS detectors. One of our primary goals for this year is to demonstrate chemical analysis on small particles, with the Al/ Al_2O_3 system being of particular interest to the semiconductor community.

During the past year, we have collaborated with several SEMATECH member companies and others to demonstrate the improved capabilities of the NIST microcalorimeter EDS using samples of industrial interest. In the near future, our implementation of a simplified telepresence microscopy and microanalysis system will allow further collaborations with the semiconductor industry in real time over the web. Further details and downloadable papers describing microcalorimeter EDS and its application to particle analysis in the semiconductor industry can be found at our web site (http://emtech.boulder.nist.gov/div814/microcal/microcal.htm).

Detailed guidance regarding instrumentation is outside the scope of the 1997 NTRS. However, strong industrial support for this effort has been registered by the SEMATECH Analytical Lab Managers Working Group.

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Interconnect and Packaging

Interconnect Materials and Reliability Metrology

Modern multilayer ULSI interconnects, composed of layered metal and dielectric thin films, must withstand severe conditions: triaxial tensile stresses due to passivation, and mechanical/thermal stresses caused by high current density. This project focuses on three areas: (1) Major failure mechanisms of conductors, electromigration and stress voiding; (2) Basic mechanical integrity of the entire interconnect structure; and (3) Microstructural processes that affect reliability.

Interconnect Reliability. This task develops, evaluates, and refines test structures, test methods, and diagnostic procedures to improve reliability of metal interconnects. Best values were developed for the resistivity of copper (Cu), from 50K to 1200 K, and for $d\rho/dT$ from published data for use in measuring electrically the geometry and relative purity of Cu interconnect lines. An inter-laboratory experiment was begun, using reliability test pattern NIST 33, to evaluate the precision of three electromigration standard test methods and several test-structure desgin options for single-level interconnects. Best practice designs for single-level and for via-type test structures to characterize electromigration in aluminum (Al) and Cu interconnects were compiled and used in the design of reliability test pattern NIST 36. Its fabrication in Al is being sought to continue inter-laboratory and other experiments and to begin the development of standards for test structures and test methods to evaluate via-type structures. A selection of Cu electromigration test structures were designed and are being fabricated by Rockwell Semiconductor Systems.

Mechanical Behavior of Interconnect Films. Piezo-actuated microtensile testers, based on NIST designs, are in use at Motorola and the Univ. of Colorado (Dept. of Mech. Eng.) for specimens 20 μm wide and larger. Present test methods must become more useful to industry in three ways: applicability to mechanically delicate dielectric films; ability to test few and sub-μm-wide specimens; and easy-to-fabricate test structures. A new probe-type tensile test technique, in development, requires only front-surface wafer fabrication steps, less extensive silicon etches, and no cutting of the substrate. Incidental damage is significantly reduced, allowing tests of small and delicate specimens. Measurement challenges include ultimate tensile forces of ~0.1 gram force (for 10 μm wide specimens) ranging down to milligram forces for smaller specimens, and sub-μm displacements.

Microstructural Influences on Interconnect Reliability. The NIST 34 test chip incorporates stress voiding structures whose designs were based on our recent experimental results: grain boundary triple junctions which favor rapid stress void growth may not necessarily favor rapid electromigration void growth. Local heterogeneities become the weak links in narrow interconnect lines, so microstructure-based studies of selectivity in local failure sites can provide: (1) accurate data for reliability models, (2) full correlations between different processing variables and the effects on performance, and (3) development of characterization methods suitable for future interconnect generations. Heterogeneous chemical segregation in aluminum alloy films was correlated to local variations in microstructure such as the I- and U-line character of triple junctions. NIST 36 is patterned with lines containing simulated defects to examine stress voiding. Collaborations are underway with TexSEM Labs, Tosoh SMD, Intel, SEMATECH, the Univ. of Michigan, and the Rensselaer Polytechnic Institute.

Interconnect reliability is at the core of the five most difficult challenges for the industry before 2006 that were identified in the 1997 NTRS, page 99.

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Test Structures for Mechanical Strain Characterization in IC Interconnects

Increasing device density in integrated circuits leads to more interconnect layers with smaller cross-sectional area and higher aspect ratio; all of which increase the probability of failure by mechanisms such as electromigration, stress migration, and delamination. This project is to develop MEMS-based test structures to measure the mechanical strain in interconnects on fully fabricated ICs.

The interconnect and dielectric layers of an IC can be thought of as laminates of a multilayer film composite. Fixed-fixed beam (FFB) test structures have recently been shown successful in measuring composite film strain in ICs. New test structures are now being developed to measure residual strain in each lamia of the composite. The key to closing the loop between the strain measurements and the determination of the mechanical stress in the interconnect layers is the measurement of the elastic modulus of the films. This effort will be focused on developing a unique apparatus, and new test structures, for the determination of the elastic modulus. The goals of the project is to develop test structures with the following salient features:

- Compatibility with fully processed ICs;
- No additional photolithographic steps required;
- A simple single-step or two-step release process; and
- Optical measurements of beam deflections.

The need for this work is specifically stated in the SIA Roadmap on page 58, "Physical ... measurements are required for implementation of statistical metrology ... test structures [for the purpose of evaluating stress in interconnects] can be MEMS fabricated using traditional silicon process technologies." Mechanical stress in interconnects is identified to effect chip reliability. The SIA Roadmap states that "Detecting, testing, modeling, and control of failure mechanisms" will be a key showstopper (Table 31, page 99).

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Thin-Film Characterization from Transmission-Line Measurement

This project develops methods to accurately measure the electromagnetic properties of low-K thin films from easy-to-perform in-situ transmission-line measurements. The project brings NIST's Electromagnetic Properties of Materials Group and the NIST MMIC Program into a collaborative effort with Texas Instruments to develop coplanar waveguide test vehicles, SEMATECH to develop microstrip test vehicles, and with DOW Chemical to investigate NIST fabricated test vehicles.

The methods are based on measurements of small printed transmission lines incorporating the materials to be characterized. They allow the dielectric constants of thin films and the conductivities of the metals used in the lines construction to be determined over broad frequency ranges. With our equipment we typically test from 50 MHz to 40 GHz.

1. **Texas Instruments- The Coplanar Approach.** In a collaborative effort with Texas Instruments we designed experiments and fabricated and tested coplanar waveguides passivated with BCB, HSQ, and SiO_2 films. The measurements convincingly demonstrate the approach. We have returned the coplanar samples to Texas Instruments for a cross-sectional analysis required to compute the dielectric constants and loss tangents of the thin films accurately from the measured data. In FY99 we will complete the analysis.

2. **IBM- The Microstrip Approach.** Only a small portion of the electromagnetic energy in coplanar transmission lines is located in the passivation layer we would like to characterize. In a joint effort with SEMATECH we have designed microstrip test structures with greater sensitivity. We have already completed testing of new low-K dielectric and copper conductors supplied by SEMATECH. We anticipate completing the analysis and other tests in FY99.

3. **Dow Chemical- Testing for Materials Manufactures.** We are using NIST's unique processing capabilities to pursue a very different approach to dielectric thin-film characterization at Dow Chemical, a major supplier of low-K dielectrics. In our collaboration with Dow we perform most of the microfabrication at NIST; Dow simply deposits and patterns the thin films on pretested circuits provided by NIST. A second set of measurements made at NIST tests for the differences in transmission-line capacitance. NIST has completed fabrication of the test coupons and shipped them to Dow. We hope to complete the testing and analysis in FY99.

In the 1997 NTRS, the use of low-k dielectric appears several times in the Potential Solutions roadmaps on pages 100-102. In the Priority of Technology Needs section (for interconnect) on page 103, it states, "It is expected that low dielectric-constant materials will have an even greater impact than low-resistance metals (on performance)." SEMATECH recently indicated to NIST that they ranked the electromagnetic characterization of thin-films a high priority need in the semiconductor industry.

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Experimental Micromechanics by e-Beam Moiré

In this project, we respond to the needs of the electronic packaging industry, for whom failure of the package is a major source of concern. We provide direct quantitative experimental verification of predicted deformations, and characterize actual failure modes to improve the usefulness of modeling and simulation in the design and manufacture of advanced electronic packaging and interconnect structures. To this end, we develop and apply the electron-beam (e-beam) moiré technique to measurement of displacements and observation of deformation at high magnification and use the observations to characterize failure modes and to verify mathematical models and simulations of microscale mechanical behavior.

In 1998 we responded to needs from Intel (AZ) and Motorola (TX) on packaging issues. Intel asked us to use our e-beam moiré technique to study thermally-induced displacements in the interconnect structure of a multi-chip module substrate. Motorola approached NIST with a concern about the flip-chip-on-board lifetimes when cycled through low temperatures. Nowhere else were they able to obtain displacement data on the sub-micrometer scale from the package thermally loaded between -55 and 120 °C, and their room temperature to 120 °C data were not providing the insight that they required. However, NIST was able to help using the e-beam moiré technique over the full temperature range of interest and that data was provided to Motorola. A comprehensive document describing the e-beam moiré method has been prepared to assist in technology transfer of this technique and is available though Ms. Drexler.

In FY99 we continue the flip-chip-on-board research in collaboration with Motorola. They have asked us to compare the thermomechanical deformations of two alternative package designs, as they seek to improve the reliability of the low-temperature package. Other areas to be addressed in this fiscal year are evaluating methods for decreasing the pitch of the grids in order to improve resolution, and exploring new means of producing grids that can withstand thermal cycling. Once the thermal cycling issue is resolved, the technique will be applied to measurements of thermal fatigue of advanced packaging structures. To create the smaller-pitch arrays that will be needed as chip and packaging technology advances, we plan to investigate the feasibility of performing lithography with our AFM, or using block co-polymers to form a regular array. The latter is a program with which we are cooperating under development at Colorado State University.

From the 1997 NTRS, page 150: "Key is development of in situ model mechanics elucidation and validation tools such as micro-moiré, nano indentation techniques, and interface fracture toughness techniques." At present, project collaborations are underway with Motorola and Intel (AZ).

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Hygrothermal Expansion of Polymer Thin Films

Polymers are widely used in electronic packaging in many applications. These include interlayer dielectrics, underfills in ball grid arrays, adhesives, encapsulants and substrates. In many of these applications, the polymer is in the form of a thin film on another material with significantly different physical properties. Knowing and predicting the dimensional changes of these films with temperature and humidity are important for modeling the performance and reliability of complex assemblies. The properties of these films can be significantly different from the material in bulk form, especially in a constrained geometry. In addition, these materials may only be available in the form of thin films. The most commonly used technique, thermomechanical analysis (TMA) has been previously demonstrated by round robin tests to be inadequate for determining these very small changes in film thickness.

This project has the primary objective of providing industry with robust measurement tools and data for characterizing the dimensional stability of polymers. In particular, the project is focused on the measurement of changes with temperature and humidity on the out-of-plane dimensions of thin films. NIST has designed, built and demonstrated a capacitance cell with outstanding sensitivity for measuring the out-of-plane expansion of polymer films. This project has four sets of activities: (1) determining the accuracy and precision of the technique applied to a variety of polymer measurements; (2) working with standards-setting bodies to explore the desirability of introducing the technique as a standard method for measuring thermal and hygroscopic expansion; (3) providing industry with materials property data on selected packaging materials; and (4) expanding the capabilities of the measurement techniques to electrically conducting material and to thinner films.

With regards to the first set of activities, in 1998 the accuracy and precision of the technique for thermal expansion measurements have been demonstrated on single crystal, <0001> oriented Al_2O_3 and on a 14 μm thick inner layer dielectric material. A full error analysis has been performed to study the limitations of the technique and has been published, along with the completed capacitance cell design plans, in an industrial conference proceeding and in a peer-reviewed journal. [1,2] Additionally, the errors propagated from the uncertainties in the humidity and PVT properties of air and water, have been evaluated and the results has been accepted for publication in a peer-reviewed journal. In the second set of activities, we have begun discussions with the chair of IPC's HDIS Test Methods Group to have this capacitance technique considered as an additional standard test method for the measurement of thermal expansion for cases in which the existing standards are inappropriate. In the course of the work, data on several materials of importance to the electronics industry, have been and will be, generated and disseminated through the appropriate venues. Finally, with regards to expanding the capabilities for measurement of thin film expansion, two projects are in progress. First, a newly designed capacitance cell is being built which will allow for measurements on conducting (e.g. metals) and semiconducting (e.g. silicon) materials. Secondly, due to the fact that the current design of the capacitance cell only allows for measurements of films between 5 μm and 1.5 cm, this capability is being extended with an x-ray reflectivity apparatus which allows for measurement of films of 1.2 μm down to the order of several hundred Angstroms.

The 1997 NTRS pinpoints on page113 "Areas of concern with the new materials and architectures are as follows: in-film moisture content, film stoichiometry, mechanical strength/rigidity, local stress (versus wafer stress), line resistivity (versus bulk resistivity), available of high frequency dielectric constant values... This project is working to introduce the measurement standards needed to describe thin polymer films used in these applications.

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[1]Snyder, C.R.; Mopsik, F.I.; "High Sensitivity Technique for Measurement of Thin Film Out-of-Plane Expansion", in AIP Conference Proceedings 449 -Characterization and Metrology for ULSI Technology, ed. D.G. Seiler, A.C. Diebold, W.M. Bullis, T.J. Shaffner, R. McDonald, and E.J. Walters (American Institute of Physics: Woodbury, NY, 1998), pp. 835-838.

[2]Snyder, C.R; Mopsik; F.I.; "A Precision Capacitance Cell for Measurement of Thin Film Out-of-Plane Expansion: I. Thermal Expansion", Review of Scientific Instruments, 69 (11), 3889 (1998).

Modular Thermal Conductivity Bridge Structures

Handling heat developed by modern IC chips is an essential step to accompany the evolution of ever-smaller feature sizes that increase the thermal power per unit area. All methods presently in wide use for estimating thermal conductivity of free standing thin films are based on transient methods which carry the advantage of much shorter measurement period, but depend critically on many conditions and assumptions that must be satisfied in order to extract the true thermal conductivity. These assumptions, as well as the experimental techniques, need to be critically evaluated and compared with an absolute method of measuring conductivity.

We have developed standard modular test structures for conductivity of thin films that can occupy only one small area of each manufactured IC wafer, allowing us to determine the thermal properties of the layers of metallization and polycrystalline silicon, as deposited in the actual manufacturing process. Conductivities within the plane and normal to the plane, and thermal contact resistance are all being investigated in the experimental process. The test structures are made by the single-metallization **MUMPS** (**m**ulti-**u**ser **m**icroelectromechanical **p**rocesses), a flexible but nonetheless limited process. Our bridges made by this process must be measured in a custom vacuum chamber to remove conductive heat loss through air between the bridge and the substrate. The final test structures will use a deeper pit between the bridge and substrate that will remove air-conductive coupling and allow use without a vacuum chamber.

The techniques developed here will also apply to measurement of conductive heat transfer in layered packaging structures carrying the ICs and interconnects. Computer software has been developed to automate the data-acquisition process, and reproducible free standing single-layer thin-film specimens have been made. The first preliminary round of measurements of thermal conductivity of thin layers of polycrystalline silicon has been completed and data analysis is in progress. A second set of different specimens has also been produced and measurements on these structures will significantly extend the work. Some of these structures will permit measurement of thermal contact resistance between layers. Interfacial thermal resistance between the film and substrate is a major factor being considered in the experimental process of measuring the conductivity normal to the plane, as well as in the behavior of the various layers of an electronic IC or package.

In the initial development of this technique to the micro-scale, infrared (IR) microscopy is used, which gives a complete temperature profile along the length of the Kohlrausch bridge structure. When the proper, most efficient design of a bridge is determined, resistive temperature measurement will be developed and used, obviating the requirement for an IR microscope, which would not be practical for use of the test structure in the anticipated production environment. Preliminary test structures using resistive thermometry at the middle of the bridge have already been made.

The effects and magnitude of thermal radiative coupling between the heated test structure and the environment are also being carefully considered in the development.

"*The task of dissipating the heat fluxes from IC chips while maintaining acceptable junction temperature is a significant challenge for semiconductor and systems manufacturers.*" ("1997 Assembly and Packaging Roadmap", *1997 NTRS*, p. 7).

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Solderability Measurements for Microelectronics

The decrease in dimensions of electronic devices has resulted in a dramatic increase in interconnect density. This development has introduced stringent new demands on solder and the soldering process and produced a need for improved solderability tests and standards. To meet this need, NIST is developing test techniques and scientific guidelines that U.S. manufacturers can use to evaluate solder and solderability of components before committing them to the production line. Both tin-lead and lead-free solder alloys are being addressed.

The availability of improved solderability test methods will lead to increased manufacturability and reliability in microelectronic devices. Such increased reliability and predictabilty for solder joints is essential for U.S. industry in producing fine pitch surface mount and ball grid array interconnects, where small size scales and limits on visual inspection of the solder joint make rework of improperly soldered connections difficult or impossible. Current work is emphasizing solders designed for high temperature application, for PWB or hybrid assemblies as well as for die attach. The reliability of lead (Pb) free and Pb-containing solders during high temperature application is also being addressed in a collaborative project with Ford, Delco, Rockwell International and various suppliers.

The growth of oxides on surfaces is a frequent cause of loss of solderability of printed wiring boards and component leads during storage. Electrochemical tests, especially sequential electrochemical reduction analyses (SERA), are being applied to measure the chemical nature of the species produced by oxidation, the structures and thicknesses of the surface layers, their role in the degradation of solderability on copper substrates, and the effectiveness of imidazole oxidation inhibitors. We have recently focused our attention on establishing an electrochemical quartz crystal microbalance (EQCM) capability which will provide an in-situ mass measurement, with sub-monolayer resolution, during the electrochemical examination of copper in solution. This will allow us to correlate the mass and the charge associated with the formation and removal of the copper oxides and may become instrumental in understanding SERA transients which the industry is currently considering as a test for determining solderability.

These solderability issues are driven by the smaller pitch and footprints of leads on BGA and surface mount devices and by concerns raised by the advent of lead-free solders which will inevitably involve changes in soldering techniques. Industry is pursuing significant pitch reduction goals for fine-pitch BGA and chip scale packages, as described in the Assembly and Packaging Section of the 1997 NTRS, Table 46 on page 142, and in Table 47 and 48 on page 143. Table 50 (p. 147) Assembly & Packaging ESH Crosscut Issues identifies elimination of Pb as a challenge yet to be met. The IPC National Technology Roadmap for Electronic Interconnections (1997) in its assembly materials section identifies improved solderability tests and lead-free solders as needs to achieve industry goals projected for the next 2 to 4 years.

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Measurements for Electrodeposited Copper Interconnects

Recently, IBM and Motorola announced that each had independently developed chip manufacturing processes based on copper metallization. The copper is deposited electrolytically and wafer planarization is achieved by chemical-mechanical polishing (CMP). Compared to the aluminum-based interconnect material currently used in integrated circuits, copper has the advantages of lower resistivity and less susceptibility to electromigration and stress migration failures. Copper can be deposited into vias and trenches with aspect ratios as high as 10:1 only when inhibitors are added to the plating bath. Within 24 hours at room temperature, the grain size of the electrodeposited copper increases by an order of magnitude and the resistivity drops by about 25%. The grain size of the copper also has a significant effect on the response to post-deposition steps such as chemical-mechanical polishing. For future generations of devices with reduced size, the kinetics of recrystallization need to be better understood.

The recrystallization of the copper results in a beneficial decrease in resistivity, but it is not clear whether the recrystallization is simply due to the fine grain size inherent in the use of additives or is also driven by the presence of impurities, especially the distribution of impurities in and around the trench. The poor understanding of the process is unsettling to the industry which is seeking optimum performance in ever-smaller interconnects. The primary objective of our research will be to understand the factors controlling recrystallization in copper electrodeposits, especially the role of additives. A proper model of the recrystallization process would help industry design the deposition conditions and subsequent sequence of processing operations such as thermal anneals to obtain the maximum performance.

Our research activities will focus on the incorporation of additives in electrodeposited copper and the correlation of the copper recrystallization kinetics to these impurities. The Electrochemical Processing Group is currently using in-situ scanning probe microscopy (SPM) to characterize the structure and dynamics of the solid/electrolyte interface and to specifically determine the role of inorganic and organic adsorbates on the evolution of thin film microstructure and morphology during growth of copper. In addition, we are establishing an electrochemical quartz crystal microbalance (EQCM) capability which will provide an in-situ mass measurement during electrodeposition with sub-monolayer resolution. This will allow us to measure, quantitatively, the amount of additives being incorporated into copper electrodeposits from several commercial plating baths. For correlation of resistivity changes with recrystallization phenomena, copper films will be formed by electrodeposition in the presence of additives and their recrystallization and resistivity changes will be monitored by X-ray diffraction (XRD) texture measurements and four-point resistivity measurements, respectively. Analysis by transmission electron microscopy (TEM) will be performed as needed. MSEL will collaborate with Dale Newbury of CSTL who will use secondary ion mass spectroscopy (SIMS) to establish and hopefully quantify the presence of C, S, N, and O impurities.

As cited on page 99 of the 1997 NTRS, the introduction of copper metallization and low dielectric constant materials should lead to a six-fold improvement in signal delay. The introduction of these new materials also represents the most difficult interconnect challenges in the near future.

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Wafer Characterization and Processing Metrology

Contactless and Nondestructive Optical Methodology for Quantifying Oxygen in Heavily Doped Silicon

The National Technology Roadmap for Semiconductors (NTRS) identifies impurity detection (particles, oxygen, and metallics) at levels of interest for starting materials as one of five metrology challenges and states "existing FTIR method must be modified for heavily doped silicon wafers". Under this new program, we plan to develop a contactless and nondestructive optical techniques including infrared reflection and Raman scattering which are capable of detecting and measuring interstitial oxygen in both heavily and lightly doped Czochralski silicon wafers

The program elements include:

1. **Fourier Transform Infrared (FTIR) Measurement Methodology.** The semiconductor industry has relied on high accuracy and precision measurements of oxygen in silicon by FTIR since the early 1970's. At that time, it was first recognized that oxygen when precipitated, results in crystal defects that entrap metal impurities away from active device junctions at the surface. In spite of the successful development of this technology over the past two decades, little progress has been made in measuring interstitial oxygen (O_i) in heavily doped silicon, the material of choice for current and future IC fabrication. The problem arises from free carrier induced reflection and absorption of infrared light in such conducting substrates. Our approach takes advantage of the fact that reflected signals are orders-of-magnitude larger than conventional transmitted signals, thereby making the measurement feasible. Initial calibration of the IR reflection intensity with the O_i concentration will be confirmed using other less efficient and destructive methods. If successful, the installed base of FTIR instruments throughout the semiconductor industry may be used with only minor modifications, and at a reasonable additional cost, to fulfill this significant materials need.

2. **Raman Scattering Measurement Methodology**. Raman spectroscopy can provide complimentary information to FTIR and, therefore, can be used to investigate many of the same systems. In addition, Raman spectroscopy offers the prospect of increased spatial resolution with respect to FTIR, the Raman microprobe being commonly employed with micron-scale spatial resolution in such applications as stress measurement in silicon. Recent technical advances have also greatly increased the sensitivity of Raman spectroscopy. We plan to take advantage of these improvements as well as the fact that, unlike transmission FTIR, the sensitivity of Raman spectroscopy is not significantly affected by the presence of free carriers.

The 1997 National Technology Roadmap for Semiconductors (NTRS) identifies five metrology challenges. One of the five specific critical metrology challenges quoted in the 1997 NTRS is the measurement of oxygen in heavily doped silicon, Table 60, page 180 (reference 2).

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Wafer and Chuck Flatness/Thickness

Limited lithographic depth-of-focus budgets for finer features combined with larger silicon wafers pose new challenges for flatness and hence for flatness metrology; distortions induced by conventional vacuum chucks are part of the problem. This project has three aspects addressing the problem: (1) interferometric measurement of as-chucked wafer flatness; (2) interferometric measurement of thickness variation; and (3) development of new polishing processes.

1. **Interferometric Measurement of As-chucked Wafer Flatness.** NIST uses a commercial Fizeau interferometer to measure as-chucked wafer flatness with uncertainties approaching 2 nm over diameters up to 150 mm. The entire wafer is imaged at once, unlike scanned-probe techniques. The method has been extended to 300 mm wafers with slightly increased uncertainty by applying a technique well known to the optics industry (the Ritchey-Common test). These results were published at the Optical Fabrication and Testing Workshop in Hawaii June 1998. The uncertainty for 300 mm apertures will be reduced with a next-generation interferometer due for installation at NIST in 1999. The NIST group uses these capabilities to evaluate specific vacuum chuck systems as well as to explore new chucking concepts. Preliminary evaluations of chuck-induced distortions for small wafers have been made. NIST is developing chucks made of hard, porous ceramics which can be made extremely flat and provide superior support of the wafer from a large number of distributed points, as well as exploring other chuck concepts.

2. **Interferometric Measurement of Thickness Variation.** The NIST team has developed and received a patent for a new technique for measuring thickness, free-standing bow, and thickness variation of semiconductor wafers. The measurement is based on infrared interferometry and can be used to evaluate wafers up to 300 mm in diameter. NIST has purchased and installed a commercial system based on this patent and is currently characterizing the instrument. Variations of the technique are being investigated to reduce measurement uncertainty.

3. **Development of New Polishing Processes.** NIST has developed and received a patent for a novel lap concept that can be applied to both diamond lapping and chemo-mechanical polishing (CMP) processes. The process can be used for rapid, low-damage lapping of crystalline substrates such as silicon and sapphire, and has been shown to reduce silicon wafer fabrication times when incorporated into current manufacturing processes. Rodel Inc. was granted a license to this patent and is developing the technology through the Center for Nanomachined Surfaces, a University-based research institution at the University of Delaware.

Conversion to 300 mm wafers will peak in 2001-2 (1997 NTRS, page 63) with site flatness (25 x 40 mm) below 100 nm by 2006 (1997 NTRS, Table 20, page 64); development of wafer preparation processes for 300 mm wafers are underway (1997 NTRS, Figure 14 on page 67, and industry contacts) and SOI may become more than a niche technology for 130 nm and beyond (1997 NTRS, page 60). Issues with CMP are discussed in 1997 NTRS pages 106 through 108.

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Fundamental Process Control Metrology for Gases

Gas pressure, composition, and flow rate are fundamental operating variables in many semiconductor fabrication processes. NIST's efforts to support the measurement and control of these important variables have two elements: First, insuring that relevant standards and calibration procedures are available and widely disseminated. Second, examining the performance characteristics of process instrumentation to permit their optimum use by industry. These efforts are focused in two areas: partial pressure measurements or residual gas analysis, and the measurement of low gas-flows.

NIST vacuum (partial-pressure) standards have been used to examine the performance characteristics of commercial residual gas analyzers (RGAs), the most flexible instruments available for insitu monitoring of process gas composition. These studies found significant performance problems for many RGAs. Subsequent experimental and theoretical work have found that the most serious problems are due to electron and ion space charge in different parts of the RGA. For most RGAs these problems can be alleviated by proper adjustment of instrument operating parameters, and techniques have been developed for the in situ adjustment and calibration of RGAs[1]. Within the past year the RGA studies have been extended to the new closed-ion-source (CIS) instruments. Initial results indicate significantly smaller anomalies than found in some of the older instruments. Within the past year NIST initiated a collaboration with the University of Maryland on the use of RGAs to control a tungsten deposition process. The objectives are threefold: To test in situ RGA-calibration procedures in a process tool, to examine the quantitative behaviour of RGAs operating under process conditions, and to examine the feasibility of using RGAs for real-time process control. Results to date with the highly reactive gases that must be measured for this process (WF_6 and HF) clearly show that we must improve instrument stability, and that process-gas sampling techniques are critical to quantitative measurements.

NIST gas-flow work has been strongly motivated by the SEMI/SEMATECH Thermal Mass Flow Meter (TMFC) Working Group. Responding to their call for improved standards for low gas flows, NIST developed standards to cover the range up to 1000 sccm with uncertainties of about 0.1%. A new standard, completed last year and currently being evaluated, will extend the range to 10,000 sccm. The transfer of NIST low-flow standards capabilities to industry has been greatly enhanced by the development of very stable (0.2%) laminar flowmeter transfer standards[2], covering the range of 1 sccm to 1000 sccm. These have been used to perform on-site proficiency tests of industrial flow standards at a number of fabrication facilities and TMFC manufacturers. As is the industry practice, NIST flow standards operate only with inert gases. However, the need for standards that will operate with reactive process gases is evident, and NIST is developing a flow standard that will be tested with corrosive gases. NIST is also experimenting with acoustic flow measurement techniques as a possible alternative to TMFCs for low flows and reactive gases[2].

Residual gas analysis (gas contaminant monitoring) is discussed in the 1997 NTRS on page 184. Fluid purity and residual matter in vacuum are discussed on page 177 and in Figure 46. Process control in relation to process sensors, such as partial pressure measurements and flow, are discussed on pages 183 and 184.

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Low Concentration Humidity Standards

Quantification of the effects of residual water vapor on semiconductor fabrication processes is seriously compromised by large uncertainties in the measurement of humidity levels at or below ≈1000 nmol/mol. Regrettably, primary methods of measurements in this range do not currently exist. This project is driven by the need to establish such primary humidity measurement standards at trace levels, thus enabling the realization of sensitive yet accurate hygrometer technology.

The project cornerstone is a thermodynamically based humidity source known as the Low Frost-Point Generator (LFPG) capable of delivering 1 μmol to 3 nmol of water vapor per mole of dry gas. This humidity level is precisely controlled through active regulation of the saturator temperature and pressure. With a temperature stability of better than ±2.5 mK, the LFPG's mean output (expressed as an amount fraction of water vapor in air) has a precision of better than ±0.05 %. In FY 98, an active pressure control system was added to the LFPG, thus making the generated humidity level independent of barometric pressure. The system is fully automated and can operate unattended for weeks at a time, as may be required for measurements at very low humidity levels. Conversely, actively controlled LFPG output can be rapidly programmed to ramp through a series of desired values; a feature enabling the efficient calibration of transfer standards over a wide range of setpoints. In FY 99 the temperature regulation system on the LFPG will be modified, a change that is expected to reduce the minimum LFPG output humidity level reduced by at least an order of magnitude.

In FY 98 a custom-designed diode-laser-based hygrometer (DLH) was incorporated into the LFPG standard. The DLH was designed as an in-line diagnostic for monitoring humidity levels in semiconductor process gases. Using the LFPG as a stable humidity source, tests of this prototype hygrometer were implemented, establishing that the DLH had background humidity levels below 2 nmol mol/mol, a dynamic range of better than 1000/1 and a resolution of better than 0.25 nmol/mol. These experiments were critical to the development of a similar DLH which is expected to be commercially available in the near future. Plans for FY 99 include using the LFPG and DLH in tandem to investigate several topics which include; the precision of industrial humidity standards, nonideal effects in water vapor gas mixtures, and the vapor pressure of ice at temperatures in the range −50°C to −100°C.

Fiscal Year 1998 saw continued development of Cavity Ring-Down Spectroscopy (CRDS) as an absolute technique for measuring water vapor concentration. A new CRDS system based on diode laser technology was designed and constructed, with the intention of measuring water vapor in process gas streams such as phosphine and similar gases that are used in the epitaxial growth of semiconductors.

As discussed in the 1997 National Technology Roadmap for Semiconductors in the chapter entitled Metrology, the evolution of sensor-based metrology for integrated manufacturing requires the development of in-situ sensors, to provide in-time data for active process control and elimination of wafer misprocessing. In Table 60 entitled Metrology Difficult Challenges, the need for robust sensor technology and impurity detection in starting materials is highlighted.

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Plasma and CVD Process Measurements

Improved characterization and control of etching and deposition plasmas are required for the next generation of semiconductor fab processes. NIST is addressing the metrology-related aspects of this problem through development of diagnostic tools and techniques on a simple yet highly-relevant reference platform. These tools probe the microscopic characteristics of the discharge, such as species densities, electron and ion energies, and optical emission characteristics.

While these parameters are the most appropriate to describe plasma conditions, macroscopic parameters (power, pressure, gas flow) are used as control parameters today because the complex relationships among the microscopic variables are uncharacterized. A major task is the development of methods to translate microscopic plasma parameters into macroscopic control parameters.

Much of this work uses a universal plasma reactor called the GEC rf Reference Cell (GEC from the Gaseous Electronics Conference where the idea was conceived). More than 25 such cells are currently in use as a standard, reproducible platform for accurate intercomparisons of experimental data and results from plasma models. The GEC cells at NIST are equipped with a wide range of diagnostics including rf current and voltage analysis, Langmuir probes, optical emission, mass spectrometry with ion energy analysis, 1-D and 2-D laser-induced fluorescence (LIF), and absorption spectroscopy

To date, these diagnostics have been applied to plasmas in Ar, He, Ne, Xe, Kr, O_2 H_2, N_2, SF_6, CF_4, CHF_3, Cl_2, BCl_3, NF_3, C_2F_6 and various mixtures of these gases. Results have identified diagnostics applicable to industrial reactors and the limits of those techniques, as well as the generation of basic plasma data suitable for the validation of various discharge models.

Examples of specific results include: (1) a complete electrical characterization of the GEC cell resulting in improved plasma reproducibility; (2) a provisional patent for a non-invasive, non-perturbing technique for measuring the ion current at wafers exposed to high-density plasmas, based upon electrical measurements; (3) development of optical tomography as a uniformity and reproducibility monitor for industrial reactors; (4) determination of neutral and ionic species in Cl_2-containing plasmas, including measurement of the degree of gas dissociation for different plasma conditions in inductively coupled plasmas; (5) measurement of CF_2 2-D spatial densities in CF_4, C_2F_6, and CHF_3 chamber cleaning and etching plasmas for investigation of plasma uniformity and model validation; (6) development of a database of fundamental electron-interaction data for plasma processing gases; and (7) development of a plasma oscillating probe for the measurement of the electron density in inductively coupled plasmas; and development of plasma uniformity control using tunable loads.

Related projects supply basic support for modeling electric discharges used in semiconductor fabrication. These include modeling of particle formation in plasma-enhanced and thermal CVD reactors, measurement and analysis of fundamental reference data for industrially-relevant gases, and dissemination of experimental results to more than 25 different laboratories using GEC cells. A web page is maintained at NIST (http://physics.nist.gov/rfcell) that contains a bibliography of over 100 papers directly related to research performed on the GEC cell, along with other critical information about the reference cell.

Future plans include: (1) development of a new reference reactor more closely resembling industrial designs; (2) development of additional sensors for plasma process monitoring and control; (3) continued measurement, assessment, and distribution (via Internet) of fundamental data for plasma processing gases necessary to model commercial reactors and processes; (4) further investigation of chamber-cleaning plasmas; (5) development of IR and millimeter wave absorption spectroscopy for process control; and (6) investigation of paused plasmas.

The degree of empiricism embodied in the plasma tools of today is so well-known that it almost escapes mention in the 1997 NTRS. For example, the needs for modeling and simulation are presented in Table 28, page 94, and the need for additional process control is presented in Table 30, page 97. The need to narrow process-induced parameter distribution is mentioned on page 61. Needs for modeling for process control for gate dielectrics are discussed on page 80. Gate etch potential solutions are listed in Figure 16, page 75, and doping potential solutions are listed in Figure 17, page 76. Etch potential solutions are discussed on page 105 and listed in Figure 25, page 106.

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Metrology for Contamination-Free Manufacturing

NIST is addressing chemistry and particle formation, growth, and transport in thermal reactors in order to develop microcontamination standards. Improvements in the currently limited understanding of the physical and chemical mechanisms responsible for the formation, transport and growth of particles in the gas phase are critical for the minimization of microcontaminants in these process reactors. The effort being undertaken here uses both measurement and modeling techniques in order to gain an understanding of these physical and chemical particle growth mechanisms. Model validation through coordinated experimentation in prototypical reactors and techniques for collating and disseminating reference data in an efficient and timely manner are both important components of this task.

A rotating disk CVD reactor for laboratory experimentation was designed and built prior to FY 1998. During FY 1998, the actual laboratory installation of this reactor was brought close to completion. This apparatus is capable of achieving a substrate temperature of 1300 K and a rotation rate of 1000 rpm. It will be possible to perform silicon chemical vapor deposition at the purity and cleanliness levels required for microelectronics fabrication. During FY 1998, initial temperature measurements were performed in the gas-phase utilizing *in situ* Raman spectroscopy. Comparisons between experimental temperature profiles and those calculated from our microcontamination model were good. Initial *in situ* spatially resolved optical measurements of gas-phase species and particle fields in this reactor will be performed during FY 1999.

A rotating disk reactor model that predicts the formation and transport of microcontaminants has been developed and awaits experimental validation. During FY 1998, the development of a second microcontamination model for this reactor was initiated. This model will utilize a more fundamental type of aerosol model requiring fewer a priori assumptions than the existing one. The use of two different types of models will provide enhanced synergy for all aspects of this numerical and experimental investigation.

The effort in the area of physical and chemical properties data for species of importance in semiconductor processing continued during FY 1998 with the near completion of the addition of thermochemical data for silicon oxyhydrides to our CKMech web site (http://www.nist.gov/cstl/div836/ckmech.html). During FY 1999, this work will be completed and chemical kinetic data (complementing the thermochemical data previously assembled) for silicon hydrides will be researched and made available.

The need for basic chemical/physical data for equipment modeling, as well as the need for model validation, are discussed in the Modeling & Simulation Section of the 1997 NTRS on page 189. The requirement for contaminant control strategies is discussed throughout the Defect Reduction Section, pages 163 through 178. Table 54 on page 164 calls for advanced chemistry/contamination models for developing defect-free, intelligent equipment. Critical particle sizes for wafer environments are defined in Table 59 on page 170. The need for a more fundamental understanding of reactor contaminant formation/transport is discussed under Process Equipment on pages 177 and 178.

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Temperature Measurement for Rapid Thermal Processing

Achieving accurate temperature measurement in rapid thermal processing (RTP) is crucial to quality control for front-end processing of silicon wafers. The goal of this inter-laboratory collaboration at NIST is to achieve ±2 °C accuracy and ±0.25 °C repeatability in radiometric temperature measurements of silicon wafers in the RTP environment. This project consists of four major elements: (1) radiometer in situ calibration using thin-film thermocouples, (2) characterization of new generation radiation thermometers, (3) characterization of wafer radiation environment, and (4) establishing industry collaboration and community support for this project.

The first task of this project is to provide an in situ, 200 mm silicon calibration wafer instrumented with thin-film thermocouples, so that the radiation pyrometers can be used in wafer processing with temperature uncertainties of less than 2 °C. We have developed and evaluated a calibration methodology to replace the wire thermocouples of current calibration wafers with thin-film thermocouples. The approach has reduced the uncertainty in present wafer technology by (1) reducing the perturbation due to heat transfer at the massive thermocouple junctions in the present technology and (2) replacing the commercial thermocouples with the superior platinum/palladium (Pt/Pd) system. We have achieved ±4 K uncertainty up to 1100 K (827 °C) using Pt/Pd and rhodium/platinum (Rh/Pt) thin films combined with Pt/Pd wire thermocouples on the calibration wafer. Further work is needed to achieve the ±2 °C uncertainty and higher calibration temperatures. The approach has three key areas of activity: (1) fabrication and evaluation of 200 mm calibration wafers with the thin-film Rh/Pt and Pt/Pd thermocouple arrays, (2) materials analysis and characterization of Rh/Pt and Pt/Pd thin-film thermocouple systems on silicon wafers using SEM, SIMS, and EDX, and (3) high temperature research up to 1300 K using other materials such as tungsten (W) and rhenium (Re).

Characterization of radiometers includes both calibration and examination for various radiometer performance criteria. Through existing CRADAs, calibration procedures for optical fiber and spot type radiometers will be investigated, and modeling and evaluation of radiometer calibration systems will be performed. In all calibrations, a thorough uncertainty analysis will be performed to achieve traceability to the International Temperature Scale of 1990. In a recent calibration, the radiometer uncertainty is less than 0.75 °C.

Modeling efforts will be divided into two parts. First, modeling of radiation from the lamps to the wafer will be investigated to try to understand the effects of the source and the chamber on the irradiation to the wafer. Second, modeling of the radiation paths to the radiometer will provide information on how much of the total radiation enters the detector system. This information can be collectively used in future experimental designs, understanding of the heat transfer phenomena, characterization of the measurement system and uncertainties, and resolution of measurement and calibration problems. The NIST modeling efforts have resulted in estimating the wafer effective emissivity for various chamber configurations and in analyzing the uncertainties in the light pipe measurements.

Industry collaboration with NIST in this project is crucial and is evident with the CRADAs and university grants that have been mentioned. On January 28th, 1999, the third annual NIST RTP Advisory Group Meeting will be held to present the status of the NIST RTP project and to gather input on the status of the RTP community. From this meeting, we have defined critical needs and areas of collaboration with NIST.

The ±2 °C uncertainty requirement in temperature measurements for RTP tools was established by the Technical Working Group on Manufacturing of the 1997 National Technology Roadmap for Semiconductors and is derived from the 1999 requirement for 0.18 μm line widths. Both the ±2 °C accuracy and ±0.25 °C repeatability requirements have been quoted from Don Lindholm's keynote address at the RTP '97 Conference. RTP is a key technology for the cluster tool, single wafer manufacturing approach that will be needed to produce ASICs and DRAMs with reduced line widths and thermal budgets.

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Particle Measurements in Support of the Semiconductor Industry

The project objective is to develop a facility for accurately measuring particle size and concentration and for depositing monosize particles on calibration artifacts to support the *National Technology Roadmap for Semiconductors* goal of quantifying 50 nm diameter particles by wafer scanners by 2006. This project consists of three elements: (1) Development of an electrospray system needed for particle calibration sizes smaller than about 70 nm; (2) Calibration measurement and related modeling for 50 nm and 30 nm particle size standards; (3) Development and testing of an electrostatic deposition facility for particles in the size range 30 nm to 300 nm.

The size distributions were measured for polystyrene latex (PSL) spheres generated by both a TSI Inc. prototype electrospray and by pneumatic nebulization. Results have been obtained for particle sizes 30 nm, 50 nm, 78 nm, and 100 nm. The electrospray eliminates the production of multipet particles and greatly reduces the thickness of the residue coating on the PSL spheres. SEMATECH has been briefed on these results and during the next year a manuscript based on this work will be written. An improved electrospray unit will be purchased next year and tested for generation rate of particles, constancy of output, and ease of use in regard to clogging.

Last year the particle size results for three monosize PSL calibration spheres of nominal size 90, 125, and 220 nm were published in the Proceedings of the 1998 International Conference on Characterization and Metrology for ULSI Technology held at NIST. Manuscripts were prepared and accepted for publication by *Aerosol Science and Technology Journal* on the effect of Brownian motion on the performance of the differential mobility analyzer and the use of a modified inlet for the analyzer. During FY1999 measurements will be made on candidate calibration spheres with sizes of 30 nm and 50 nm in regard to their suitability as calibration standards.

The particle deposition work supports Thomas Germer's project on "Optical Scattering for Wafer Surface Metrology." A low pressure cascade impactor was used for depositing monosize polystyrene spheres of sizes 100 nm, 180 nm, and 220 nm on 2.5 cm diameter silicon wafers. A manuscript describing the deposition method and the light scattering results entitled, "Polarization of Light Scattered by Particles on Silicon Wafers," was presented at the SPIE Meeting in January, 1999. Limitations of the existing deposition method are low collection efficiency for particle sizes of 100 nm and less and non-uniform deposits. During the next year, an electrostatic deposition facility will be developed and tested for collecting the charged PSL spheres exiting the differential mobility analyzer.

Particle contamination appears throughout the Crosscutting Working Group on Defect Reduction in the 1997 NTRS. Table, 57 page 167, indicates that there is no known solution for the 2006 goal of detecting 33 nm PSL spheres on bare silicon wafers.

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Optical Scattering for Wafer Surface Metrology

Optical scattering inspection tools are indispensable in modern fabrication lines for locating and sizing particles and defects on silicon wafers. As feature sizes decrease and aspect ratios increase, the requirements for the detection of defects and contaminants become tighter. This program focuses on developing a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, and characterize the response of instrumentation to different types of defects. The program elements include:

1. **Polarized Light Scattering Measurements.** The Goniometric Optical Scatter Instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV). We demonstrated that measurements of the polarization of scattered light, coined *bidirectional ellipsometry*, allow different scattering mechanisms to be distinguished. To fully develop this technique, we measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, or patterns, all with or without dielectric layers. The emphasis is on providing accurate data which can be used to guide the development of light scattering instruments, and to test models for light scattering.

2 **Theoretical Light Scattering Calculations.** The focus of our theoretical work is on (a) developing models that accurately predict the polarization of scattered light, and (b) determining what information can be efficiently and accurately extracted from light scattering measurements. Simple models, such as those based upon the Rayleigh approximation, are used in conjunction with more complex finite element time-domain and discrete-dipole approximation techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare wafers, and (c) scattering by high aspect ratio vias.

3. **Instrument Development.** A second instrument, the Scanning Optical Scatter Instrument (SOSI) complements the capabilities of GOSI as a prototype for a production-line light scattering inspection tool. An instrument with twenty-eight fixed detection elements covering the scattering hemisphere, SOSI enables a determination of the differential scattering cross section, for individual particles or defects on a wafer surface. This instrument can be configured so that it is blind to interfacial roughness, allowing a factor of two decrease in detectable particle diameter. Together with an understanding of the light scattering functions for different imperfections, SOSI has a substantially improved capability for rapidly detecting and identifying defects, particles, and microroughness on wafers.

Defect detection plays an important role in maintaining high production yields on fabrication lines. Defect detection needs are mentioned throughout the 1997 NTRS, with specific detection requirements outlined in Table 57 on page 167.

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Thermophysical Property Data for Modeling CVD Processes and for the Calibration of Mass Flow Controllers

This Project will produce a data base for the thermodynamic and transport properties of the gases used in semiconductor processing. The data will be used for equipment modeling in chemical vapor deposition (CVD) processes and they will provide a rational basis for transferring the calibrations of mass flow controllers (MFCs) from surrogate gases to process gases.

The Fluid Science Group will determine the heat capacity, thermal conductivity, viscosity, diffusion constants, and the pressure-density-temperature relation $P(\rho,T)$ of process gases, surrogate gases (used to calibrate MFCs), and mixtures of process gases with carrier gases (used in CVD processes). The results will be disseminated as a data base. Early experimental results will range up to 473 K and from 25 kPa to 400 kPa (or to 80% of the vapor pressure for condensable gases); later results will reach higher temperatures. Physically-based methods for extrapolating the results to the high temperatures typical of CVD processes will be developed.

The MFC Working Group identified seven gases as having the highest priority. They are the process gases Cl_2, HBr, BCl_3, WF_6, and the surrogate gases CF_4, SF_6, and C_2F_6. These will be studied first.

The National Technology Roadmap for Semiconductors identifies "Equipment Modeling" as first in a list of "Technology Requirements" and states that "the drivers for equipment modeling are equipment design, process control, . . . " The Roadmap indicates that continuing research is needed to obtain experimental data for "transport and thermal constants."

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Lithography

Radiometric Metrology for Deep Ultraviolet Lithography

The National Technology Roadmap for Semiconductors identifies improvements in photolithography technology as a critical requirement for shrinking IC feature sizes below the present 250 nm generation. Two key issues are the tightening of photolithography exposure control and the extension to shorter wavelengths. The tightening of exposure control requires improved measurement of absolute dose and uniformity at the wafer. We are addressing this issue by investigating new stable UV source and detector standards, and developing more accurate radiometric scales. Extension of photolithography exposure wavelengths from the present-generation 248 nm to 193 nm and 157 nm requires accurate measurements of the optical properties of the materials to be used as the optical elements of the photolithographic steppers at these shorter wavelengths. We are making accurate measurements of the refraction indices and their thermal coefficients at these wavelengths of fused silica and calcium fluoride, and investigating materials issues such as strain and exposure damage that affect these properties.

The program elements include:

1. **Source Standards.** The NIST Synchrotron UV Radiation Facility (SURF II) acts as the primary standard for both sources and detectors in the deep ultraviolet (DUV) spectral region. The upgraded facility (SURF III), which includes an increase in electron energy to allow useful emission of radiation down to 2 nm, an enhancement in absolute current determination, and the addition of two new radiometric beamlines, has been completed as of January 1999. Efforts are underway to use this facility to achieve a 0.1% standard uncertainty of UV irradiance from 3 nm to 400 nm, and will enable accurate, direct radiance, and irradiance comparisons with new as well as existing source transfer standards.
2. **Detector Calibrations.** Monochromatized radiation from the recently upgraded SURF III along with an absolute cryogenic radiometer will be used to provide absolute detector-based radiometric calibrations in the spectral range from 125 nm to 320 nm with an uncertainty lower than 1%. This facility will also be used to measure the degradation in the diodes induced by exposure to UV radiation at 193 and 157 nm and efforts will also be made to measure transmittivities of fused silica and calcium fluoride at these wavelengths. Efforts are underway of characterizing degradation in diodes to 193 nm and 157 nm excimer radiation.
3. **Index Measurements.** Collaborating with MIT Lincoln Laboratory on a SEMATECH sponsored 193 nm stepper demonstration project, we have used a goniometric refractometer to measure the refraction index near 193 nm (with an accuracy of 7 ppm), as well as the dispersion and temperature dependence, for several grades of fused silica and calcium fluoride. These measurements are needed for the design of the stepper optics. With instrumentation modifications enabling operation in an oxygen-free environment, we have begun similar measurements on calcium fluoriude at 157 nm. These are needed for the design of the optics for future-generation 157 nm steppers. We have also designed and built a refractometer, based on a DUV Fourier transform spectrometer, capable of an improved accuracy of 1 ppm.
4. **Index Issues.** Compaction, bulk strain, and impurities in available grades of fused silica and calcium fluoride present problems limiting their suitability for use as optics at 193 nm and below. Our measurements of fused silica have revealed index differences between grades due to these defects. We have also identified significant strain-induced birefringence in candidate grades of calcium fluoride. We are developing optical techniques to investigate and quantify defects, compaction, and strain in fused silica and calcium fluoride, and will work with suppliers to ameliorate these problems.

The expectation that 193 nm lithographic systems will be primary patterning tools for the 180 nm and possibly down to the 100 nm generations is discussed in the Lithography Section of the 1997 NTRS, and summarized in Figure 18 on page 89. Improved radiometric and optical materials metrology are needed for the development of 193 nm systems in order to meet the requirements detailed in Table 24 on page 85.

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Deep Ultraviolet Laser Metrology for Semiconductor Photolithography

Since the first edition of the National Technology Roadmap for Semiconductors (NTRS) in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a shift towards shorter laser wavelengths in the optical lithography process. It is clear that DUV lasers, specifically KrF (248 nm) and ArF (193 nm) excimer lasers, are the preferred sources for high resolution lithography at this time. To meet the laser metrology needs of the optical lithography community, the NIST Optoelectronics Division has developed primary standards for laser energy and power measurements at 193 and 248 nm.

Presently, NIST provides 248 nm and 193 nm laser power and energy measurement services to the semiconductor community with approximately 1 % uncertainty. Recent round robin results demonstrated an offset in DUV transmittance between laser ratiometric and spectrophotometric methods, presumably due to laser cleaning of the samples. Therefore, reference transmittance measurements of optical materials at 248 nm and 193 nm, using the laser ratiometric method are now available at NIST upon request.

In addition to existing DUV laser measurement services, there is increasing demand for laser dose, i.e., energy density, measurements. Accurate laser dose measurements are important because small area detectors are widely used to monitor laser energy at the wafer plane of a lithographic tool. Accurate measurements of laser dose are especially crucial to the development of new mask and resist materials at 248 and 193 nm, since lower dose requirements can translate directly into higher throughput and extend the lifetime of an exposure tool's optical components as well.

Currently, NIST is developing new laser dose transfer standards and calibration procedures to provide improved measurement accuracy for the end user. One difficulty associated with dose calibrations is the angular response of the detector. Typically, dose meters are calibrated using a parallel laser beam with a uniform energy density. However, with the move toward variable numerical aperture lithographic tools, significant measurement errors can be introduced when extrapolating a value for laser dose with the assumption of a cosine function for the dose meter angular response. Measurements of dose meter angular response functions have recorded 40% deviations from a cosine response function [Ref. Cromer, C. L. and Bridges, J. M., "NIST Characterization of I-Line Exposure Meters," SEMATECH Technology Transfer Document, No. 91040516A-ENG (1991)].

The primary objectives of the DUV Laser Radiometry project are as follows:

1. Provide calibration services for excimer laser energy and power at 248 nm and 193 nm;
2. Provide reference transmittance measurements of optical materials at 248 nm and 193 nm;
3. Develop calibration services for dose meters at 248 nm and 193 nm; and
4. Develop improved energy and dose transfer standards appropriate for calibration transfers and accuracy improvement in the semiconductor industry.

According to the 1997 NTRS, optical lithography using 193 nm technology may be viable through 2005, Table 18 on page 89, and non-optical technologies will be available after that to extend beyond the 100 nm generation. NIST is participating in the International SEMATECH and MIT Lincoln Laboratory collaboration project on 193 nm photolithography in an effort to provide needed critical data and measurement support as quickly as possible. One critical requirement that has been identified by both MIT Lincoln Laboratory and International SEMATECH is the availability of calibration services for 193 nm laser energy meters by June 1998. This requires the development of a 193 nm primary standard, a calibration facility, and appropriate transfer standards to transfer calibrations to the industry customers. Furthermore, the 1997 NTRS has identified the need for more process control in the wafer plane, Table 22 on page 74. This requirement anticipates the need for improved laser dose metrology which can only be accomplished through the development of highly accurate primary standards, transfer standards having both high stability and radiometric accuracy, and a calibration facility to provide the means to calibrate these transfer standards and customer-supplied laser detectors.

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Design

Metrology for Simulation and Computer Aided Design

Compact Device Electrical Models: Only recently has there been a significant effort in developing an infrastructure for validating the performance of compact models. An example of this activity is the NIST/IEEE Model Validation Working Group, founded in 1994 and now having over 200 members from 100 different technical organizations. This group's activities are discussed on its Web page at http://ray.eeel.nist.gov/modval.html.

This working group has proposed two model validation standards projects that have been approved by the IEEE Standards Board: IEEE standard P1464 for Insulated Gate Bipolar Transistor (IGBT) Circuit Simulator Model Validation and IEEE standard P1485 for Micro-electronic MOSFET Circuit Simulator Model Validation. The EIA Compact Model Council (formerly the SEMATECH Compact Model Council) has also joined the NIST/IEEE Working Group on Model Validation in the development of the Micro-electronic MOSFET model Validation Standard. The first draft of this standard was completed and posted on the Working Group web site.

In addition to founding and supporting the NIST/IEEE Working Group on Model Validation, NIST has extensive laboratory efforts in this area. A test bed has been developed for validating the electrical performance of compact Insulated Gate Bipolar Transistor (IGBT) models for both hard and soft switching conditions. This test bed has been applied to evaluate the IGBT component libraries in commercial circuit simulators. As a result of this validation study, a major circuit simulator software vendor has made changes that substantially improve the accuracy of their IGBT component library for hard switching conditions and model improvements have been identified for simulation of soft switching conditions.

Compact Package Electrical Interconnect Models. An effort has recently been undertaken to develop systematic methods for including the effects of package interconnect parasitics into circuit and system simulation. Interconnect structures are becoming a dominant factor in limiting the performance of modern computer, communication, and power systems. The Time Domain Reflectometry (TDR) technique is being applied to characterize various semiconductor interconnect systems, multi chip modules, and discrete packages. Appropriate test fixtures are being developed to launch the TDR signal in a configuration that represents the application condition for the interconnect being measured, and methods are being developed to reduce the complexity of the interconnect models by accounting for the range of application conditions that a particular interconnect model must simulate accurately. Also, finite element interconnect simulation tools are being used to validate the compact interconnect models developed using the experimental TDR method.

Device and Process Simulation Benchmarking. Various efforts involving benchmarking device and process simulators are being conducted in collaboration with the EEEL SED Scanning Capacitance Metrology Project. For example, UT-MARLOW simulations were performed to calculate two-dimensional 50 keV boron implant profiles in the vicinity of a mask edge. The simulation results were correlated with scanning capacitance microscopy (SCM) measurements of the 2-dimensional profiles. Simulations are currently under way to use UT-MARLOW and TSUPREM4 to calculate two-dimensional boron profiles after implant and anneal for comparison with SCM measurements. This process will be investigated as a method to calibrate process simulator implant and anneal models using SCM measurements.

Metrology and modeling of packages are both discussed on page 132 of the 1997 NTRS. NIST has long been a strong contributor on these topics. The wide divergence between power levels for hand-held vs. high-performance applications as discussed in Table 37 on page 115 underscores the need for improved package designs as described on page 136. These can only be obtained with the aid of improved 3D models and the necessary data on materials properties to support them.

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Appendices

Appendix A: Abbreviations and Acronyms

AFM, atomic force microscope
ALMWG, Analytical Lab Managers Working Group
ASME, American Society for Mechanical Engineers
ASTM, American Society for Testing and Materials
BRDF, bidirectional reflectance distribution function
C-AFM, calibrated metrology AFM
C-V, Capacitance-Voltage
CCD, charged coupled device
CD, critical dimension
CFM, contamination-free manufacturing
CMOS, complementary metal-oxide semiconductor
CMP, chemo-mechanical polishing
CRADA, Cooperative Research and Development Agreement
CRDS, cavity ring-down spectroscopy
CVD, chemical vapor deposition
DIN, Deutsches Institut für Normung
DUV, deep ultraviolet
EELS, Electron Energy Loss Spectrometry
EIA, Electronics Industry Association
GEC, Gaseous Electronics Conference
GIXPS, grazing incidence X-ray photoelectron spectroscopy
GOSI, goniometric optical scatter instrument
IEEE, Institute of Electrical and Electronics Engineers
IGBT, insulated gate bipolor transistor
IPC, Institute for Interconnecting and Packaging Electronic Circuits
ISO, International Organization for Standardization
JEDEC, Joint Electron Device Engineering Council
LFPG, low frost-point humidity generator
MIT, Massachusetts Institute of Technology
NIST, National Institute of Standards and Technology
NSMP, National Semiconductor Metrology Program
NTRM, NIST Traceable Reference Material
PEVCD, plasma enhanced chemical vapor deposition
PPM, scanning proximal probe
RGAs, residual gas analyzers
RM, reference material
RTP, rapid thermal processing
SBIR, Small Business Innovation Research program
SCM, scanning capacitance microscope
SEM, scanning electron microscope
SEMATECH, SEiconductor MAufacturing TECHnology
SEMI/SEMATECH, Semiconductor Equipment and Materials International/SEmiconductor MAnufacturing TECHnology
SEMI, Semiconductor Equipment and Materials International
Si, silicon
SIMS, secondary ion mass spectrometry
SiO_2, Silicon dioxide
SOI, silicon-on-insulator
SOSI, scanning opitcal scatter instrument
SPM, scanning probe instruments
SRM, Standard Reference Material
TCAD, technology computer aided design
TEM, transmission electron microscopy
TDDB, time-dependent dielectric breakdown
TDR, time domain reflectometry
TMA, thermomechanical analysis
UV, ultraviolet

Appendix B: Key Words Index

(The key words correlate with the project numbers listed within the Table of Contents.)

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Appendix C: Publications

Listed below are NSMP Project-related publications from calendar year 1998. Thse NSMP project related publications, as well as those dating back through 1990, are also included within the *NIST List of Publications 103, National Semiconductor Metrology Program, and the Semiconductor Electronics Division, LP 103,* March 1999.

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